WALAILAK JOURNAL
Applied Sciences
http://wjst.wu.ac.th https://doi.org/10.48048/wjst.2021.23974

A Low Noise High Input Impedance Chopper-Stabilized Biopotential Amplifier with Ripple Reduction Technique

Ankit ADESARA[*] and Amisha NAIK

Institute of Technology, Nirma University, Ahmedabad, India

(**[*]Corresponding author's e-mail: adesara.ankit@gmail.com**)

Received: 27 January 2021, Revised: 20 May 2021, Accepted: 18 June 2021

Abstract

Biopotential signals are created as a result of the electrochemical activity of the many cells that comprise the nervous system, and they represent both normal and pathological organ function. These signals must be identified with extreme caution because they are surrounded by a great deal of noise when detected by sensors. This article explores a novel biopotential amplifier that incorporates the chopper stabilization technique to increase noise performance and minimize offset. However, by introducing the chopper modulator into the proposed design, the amplifier's overall input impedance was lowered, which was then increased to greater than 200 MΩ by adding the forward auxiliary path to the input branch. Additionally, the output ripple, produced due to switching activity and up-sampling, was reduced by inclusion of the R-C ripple removing block at the output of the operational transconductance amplifier (OTA). The designed architecture had a mid-band gain of 40dB with a power consumption of 9 µW and an offset of 10µV and a CMRR of 82 dB. It generated a noise of 42nV/√Hz. Also, the obtained results were compared with a conventional amplifier. The proposed design was verified by carrying out simulations using 180nm technology parameters. Cadence Virtuoso (Schematic editor), Spectre (Simulator), Symica and Magic (Layout) tools were used to complete the implementation and simulation of the proposed design.

Keywords: Biopotential amplifier, Chopper stabilization, Electrocardiogram, Noise, Ripple

Introduction

Biopotential signals are normally low-frequency and low-amplitude signals.As a result, it becomes crucial for the designer to mitigate power, noise and gain requirements [1,2]. These signals typically have the characteristics of low frequency and smallamplitude typically 50MHz - 250Hz and 5 µV to 8 mV for ECG signals, 0.5 - 10Hz and 1µV to 250µV for EEG signals and signals like EP and EMG carry low frequencies up to 5 kHz and small amplitudes up to 10mV. Our particular interest is to record or monitor the behaviour of EEG and ECG signal.

As there are 2 types of noises present, such as flicker noise and thermal noise, the designer must ensure that the Signal to Noise Ratio (SNR) requirements are met. Noise and interference hampered signal acquisition due to the signal's low amplitude. Also, these signals have a very low frequency, so that the design with CMOS (Complementary Metal Oxide Semiconductor) technology is very critical as it consists of dominant flicker (1/f) noise [3]. As a result, various circuit techniques, such as increasing the gate area of input transistors, using a pMOS device as an input transistor of amplifiers, auto zeroing, and chopping are used to reduce noise. However, today's chopper stabilization method plays an important role in significantly reducing noise [4]. In this technique, the OTA offset and low-frequency noise are up-converted by chopper switches to a higher frequency so that by using a low pass filter it can be easily filtered out [5,6].

A specific biopotential monitoring system consists of sensors, amplifiers, digital processing systems, and RF devices [4]. The utilization of power for each block becomes important to minimize the total power dissipation of the system as most of the power is consumed in the analogue front-end readout circuit for any recording system, especially in OTA [7]. The block diagram of the acquisition system is shown in **Figure 1**.

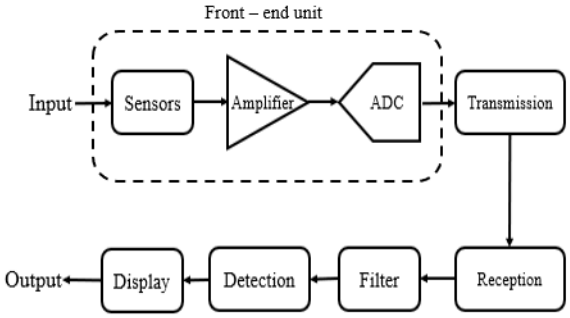

Figure 1 Block diagram of the acquisition system.

Figure 2 depicts the basic diagram of chopper stabilization, which depicts the various elements required to perform the operation, such as the chopper modulator, OTA, and low pass filter.

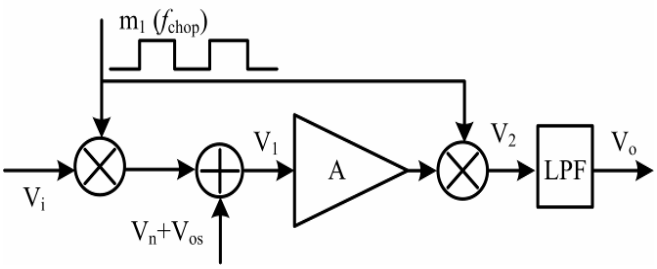

Figure 2 Chopper stabilization technique.

Due to electrochemical reactions at the electrode-tissue interface, the tissue has different DC levels at the electrodes [7]. The voltage difference is termed as DC offset and it must be reduced. To reduce the noise, different circuit techniques such as pMOS - input amplifiers, increasing the gate area of input transistors, auto zeroing and chopping are used to reduce the noise [2]. Yet, nowadays, the chopper stabilization method plays an important role in reducing noise in a significant way [4]. In this technique, the OTA offset and low-frequency noise are up-modulated by chopper switches to a higher frequency so that by using a low pass filter it can be easily filtered out [8].
The next section discusses a traditional chopper amplifier and the challenges that arise when using conventional amplifiers. Finally, the outcomes of the developed architecture are compared to the present state of the art in the literature, including all necessary simulation and analysis.

Materials and methods

In this section, the basic methodology for the proposed design, which includes the coneventional chopper amplifier and its design considerations, issues with conventional chopper amplifiers, and proposed amplifiers are presented.

Conventional chopper amplifier

Figure 3 depicts a conventional chopper amplifier that is an AC-coupled amplifier in this section. This amplifier includes a modulator, an OTA, a demodulator, and a clock generator that does not overlap. It also includes input capacitors for offset reduction and an R-C feedback network to create a high pass pole in the overall design for more stable operation [9]. In following subsection, the general consideration for finding the important parameters regarding the amplifier is mentioned. Also, these considerations are important for finding the appropriate chopping frequency and feedback parameters. Nevertheless, some parameters like CMRR, input impedance, and NEF (Noise Efficiency Factor), have to be taken care of while designing such an amplifier as those parameters are affected due to the chopper stabilization method [7].

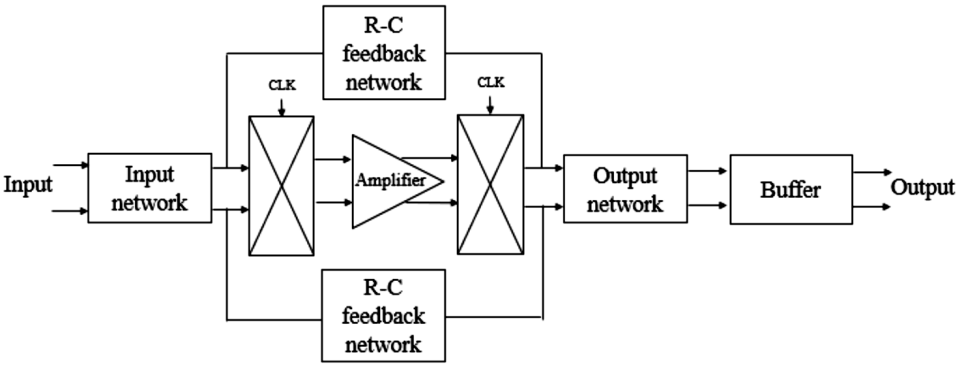

Figure 3 Conventional chopper amplifier.

The general mathematical considerationsare shown below for this amplifier.

General mathematical consideration

The closed-loop gain of design is a by-product of open-loop gain with feedback gain or factor,

$$LG(S) = \frac{A_{ol}\left(s+\frac{1}{R_2C_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)}{C_1\left(s+\frac{1}{R_pC_1}\right)\left(s+\frac{G_m}{C_{out}}\right)} \quad (1)$$

A_{ol} is open-loop gain of the amplifier which is given by,

$$A_{ol} = G_mR_{out} \quad (2)$$

The closed-loop response of the designed architecture is given by H(S),

$$H(S) = \frac{A_ms}{\left(s+\frac{1}{R_2C_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)} \quad (3)$$

The mid-band gain of the conventional architecture is defined by the ratio of input capacitance and feedback capacitance

$$A_m = \frac{C_1}{C_2} \quad (4)$$

Also, the cutoff frequencies for the high-pass band is given by,

$$\omega_{LCF} = \frac{1}{R_2C_2} \quad (5)$$

$$\omega_{HCF} = \frac{G_m}{A_m C_{out}} \quad (6)$$

While designing the chopper amplifier, parameters like power, noise, offset, input impedance, CMRR, and output ripple are to be optimized. In the following subsection, the basic issues related to the chopper amplifier are discussed.

Issues in conventional chopper stabilized biopotential amplifier

The main issue with the conventional method is the large area of input capacitors that are used to block DC so that the DC offset can be reduced and the high pass filter pole with a gain of 100 can be formed. But due to these large capacitors, the input impedance also decreases as per Eq. (6)[3].

$$Zin = \frac{1}{2C_{in}F_{chop}} \quad (7)$$

Also, the parasitic impedance is formed which is parallel to the input impedance due to the chopper modulator at the input branch, which has a finite value. So, the input impedance is further reduced as shown in **Figure 4.**

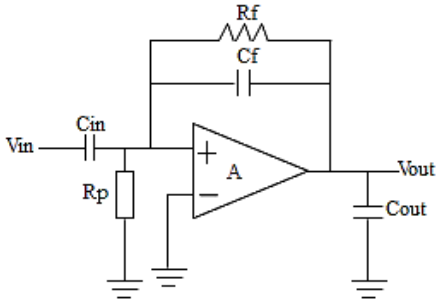

Figure 4 Parasitic input impedance.

Also, as per Eq. (7), it shows that by reducing the gain, the noise multiplication factor K is increased. So, Cin makes larger to reduce the input noise, but due to that, the input impedance is reduced further.

$$V_{in.n}^2 = V_n^2 . K \quad (8)$$

where $K = (1 + \frac{1}{A_m})$

Using the chopper amplifier, the flicker noise is reduced but the up-sampling of flicker noise and offset takes place as they are modulated once by the chopper modulator, which causes the ripple at the output. A ripple-reduction feedback loop is used in Fan *et al*.[10], where the ripple at the output of the OTA is down-converted and used as an input to the integrator. The output of the integrator is added to the output of the OTA, thus creating a negative feedback loop, which nulls the output ripple. In Xu *et al*. [11], in which the calibration takes place to compensate for the current using a D/A converter to nullify the offset and this current is given to the output of an amplifier, thus creating the negative feedback which reduces the ripple. In Burt and Zhang[12], the switch capacitor notch filter was introduced to reject the ripple. All such kinds of methods introduce switched capacitors into the feedback loop for ripple rejection, which is quite complicated to design.

The current state of the art in the acquisition system has successfully met the requirements for power and noise, but there is a significant performance gap in input impedance and output ripple. In the following section, the proposed amplifier is discussed, which also introduces the technique for increasing the input impedance and reducing the output ripple.

Proposed chopper amplifier

The chopper-stabilized biopotential amplifier offers a lower input impedance and a more substantial amount of output ripple than a conventional chopper amplifier, as discussed. Hence, in a conventional block diagram, 2 additional blocks are proposed. These are 1 forward path and 1 R-C block as shown in **Figure 5**. The detailed work of these 2 blocks is given in sections A and B. As a result, the improved version is capable of recording the signal with high input impedance, low DC offset and reduced ripple at the output while consuming less power and producing lower flicker noise.

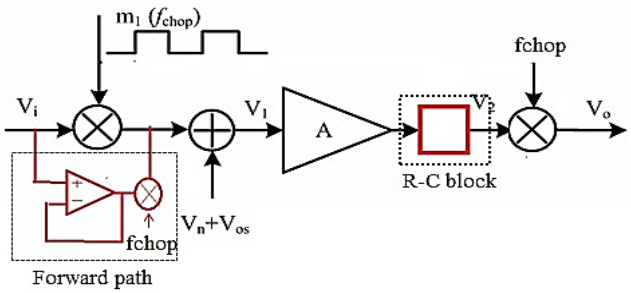

Figure 5 Modifications in conventional amplifier.

The core of this amplifier consists of OTA, which is labelled as 'A' in **Figure 5**. The schematic of OTA is shown in **Figure 6**, which is a folded cascode amplifier with an additional CMFB block to maintain the CM level at the output. The mid-band gain of OTA is set at 100 by selecting a ratio of Cin (=10pF) and C_f (=0.1pF). The bias current of this OTA is set at 3µA.

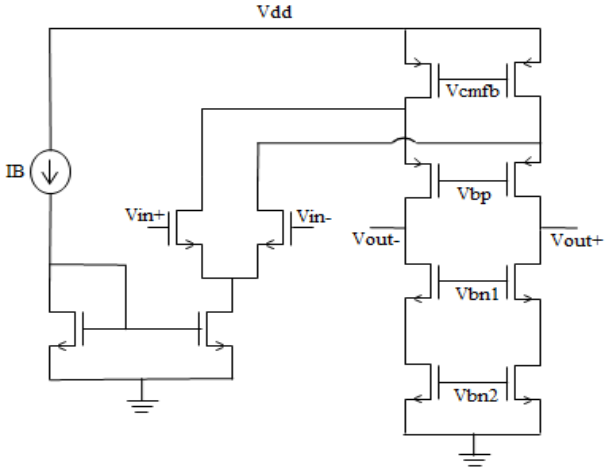

Figure 6 Folded cascode OTA.

The technique to boost input impedance

The input branch is shown in **Figure 7**. For a DC input given input voltage Vin and an externally applied clock signal fchop with input capacitance Cin, the input impedance Zin is given by,

$$Z_{in} = \frac{1}{2C_{in}f_{chop}} \quad (9)$$

where, Cin is input capacitance and fchop is chopping frequency.

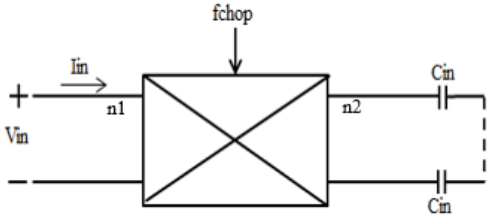

Figure 7 Input branch of the biopotential amplifier.

Here, the input impedance will be a maximum 50MΩ, if Cin is considered as 10pF and fchop is considered as1kHz, which is low for the analogue front-end for biomedical applications. So, in this implementation, to increase the input impedance of the order to at least >100MΩ, another way is through reduction of DC input current. As shown in **Figure 8**, the other forward-path is introduced to precharge the capacitor such that the potential difference between node n1 and n2 is towards zero and hence, Zin is increased by keeping the balance between Cin and fchop.

In **Figure 8**, the modified input branch with the addition of a forward-path is shown.

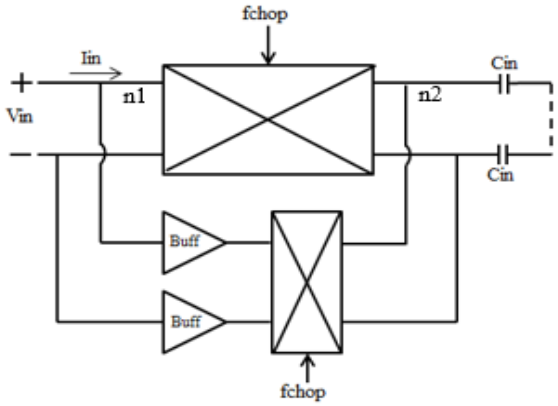

Figure 8 Modified input branch.

Using such a technique increases both the area and the power consumption. However, by carefully selecting the bias current of a forward path buffer as little high gain and frequency is required, increasing the power consumption is negligible. Here, the bias current for a buffer is taken as 1 μA.

Reduction in output ripple

The chopper-stabilized capacitive feedback amplifier is also modified for ripple rejection as shown in **Figure 5**. Due to up-modulation of the offset, the output of the amplifier has an introduction of ripple and it must be reduced. So, at output branch of the amplifier, the DC block is added as shown in **Figure 9**.

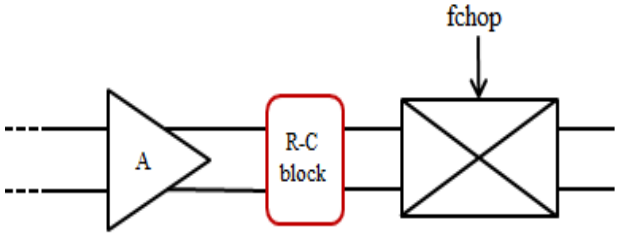

Figure 9 Modified output branch of an amplifier.

In the DC block, the R-C circuit is tuned such that it will be a short circuit at chopping frequency and an open circuit at low frequency. By such a technique, the ripple is reduced without using any additional active elements.

Results and discussion

This section depicts the biopotential amplifier's implementation. **Figure 10** depicts the overall implemented schematic diagram. Following that, the individual blocks with their schematic diagrams are discussed along with their simulation results, and finally, the overall diagram layout is shown.

Proposed implemented chopper amplifier

In **Figure 10**, the schematic diagram of the proposed amplifier is shown in which the forward path and R-C impedance circuits are added to boost input impedance and reduce ripple, respectively.

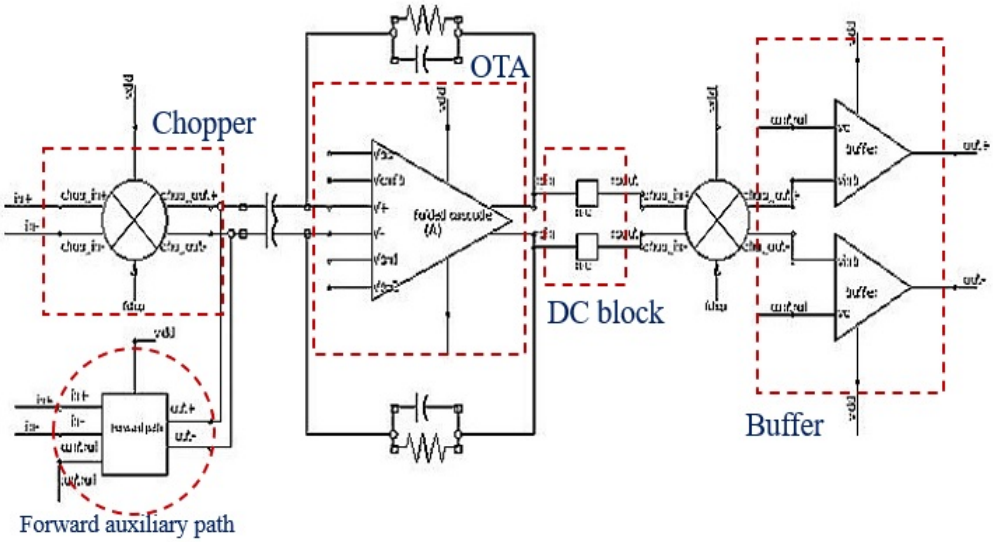

Figure 10 Schematic diagram of the proposed biopotential amplifier.

As shown in the proposed amplifier, the different subblocks are integrated to create an overall amplifier, such as chopper, folded cascode OTA, buffer, forward path and R-C impedance network. In the next subsection, the implementation and simulation of each block are discussed.

Operational transconductance amplifier (OTA)

The OTA is the heart of the designed amplifier. Here, the folded cascode OTA is designed to achieve proper gain and high output impedance so that there is no need for an extra low pass filter on the output side and, thus, the overall power consumption can be reduced. In **Figure 11**, the schematic of the OTA is shown.

The selection of folded cascode OTA is based on the comparison of different OTAs and as per the desired application from different kinds of literature. Also, for more noise optimization, instead of nMOS input devices, pMOS devices can be used.

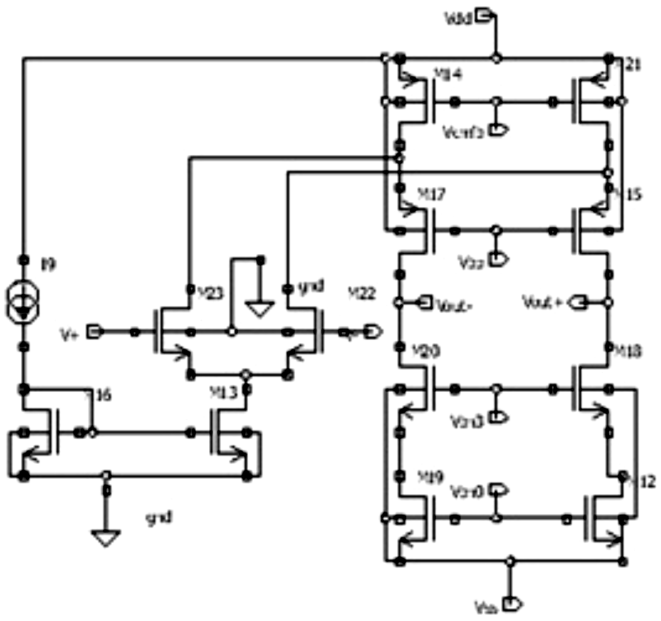

Figure11 Folded cascode OTA.

With this OTA, the common-mode feedback (CMFB) circuit and the biasing circuit for a given amplifier are shown in **Figures 12** and **13**,respectively.

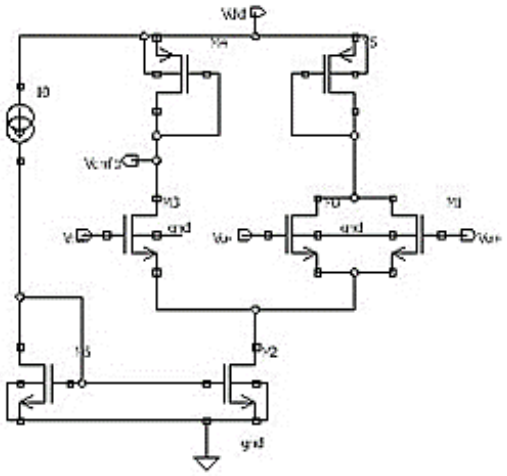

Figure 12 CMFB circuit.

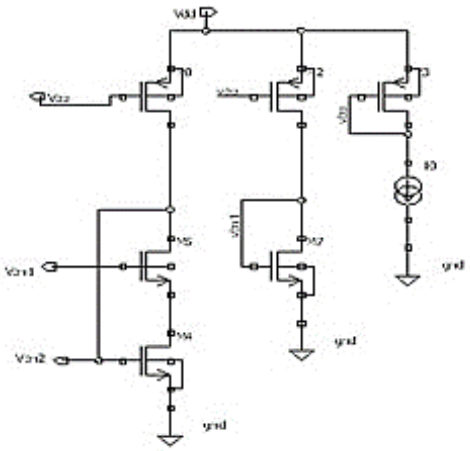

Figure 13 Biasing circuit.

The biasing circuit is needed to ensure the work of each transistor in the saturation region. In this OTA, the gain is 40dB, power consumption is 5.4μW and the noise is 31nV/$\sqrt{\text{Hz}}$. Also, the offset is 40mV and the total layout area of the design is 279.8×177.1μm^2. These are well suited for the current state of the art of recording bio-signals.

In **Figures 14** and **15** the AC analysis and the transient analysis of OTA are shown, respectively.

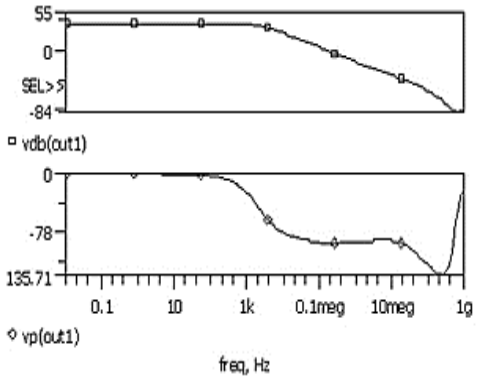

Figure 14 AC analysis of OTA.

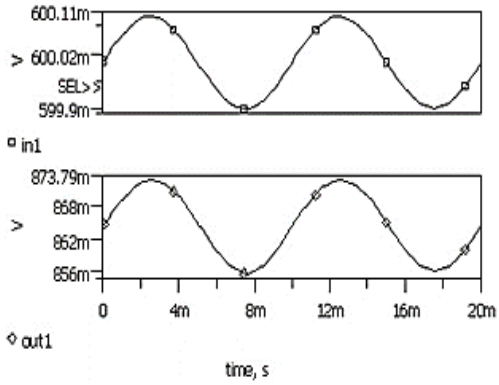

Figure 15 Transient analysis of OTA.

Chopper modulator

The chopper modulator with the nMOS switches is used in this design as shown in **Figure 16**. To operate the nMOS switches, 2 non-overlapping clocks are generated with the clock generator circuit shown in **Figure 18**with a chopping frequency of 1 kHz. In **Figure 17**, the transient analysis of a chopper is shown.

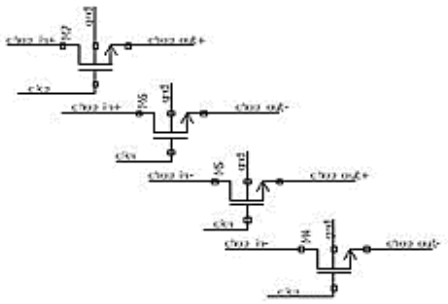

Figure 16 Chopper modulator.

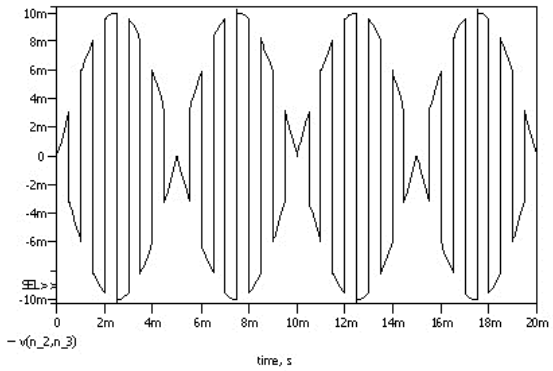

Figure 17 Transient analysis of chopper.

As shown in **Figure 18**, the clock generator circuit is designed by NAND gate and an inverter which generates the non-overlapping clock which is required to operate the nMOS switches.In **Figure 19**, the result of the clock generator is shown. In which the 2 non-overlapping clocks are generated at a frequency of 1kHz which is considered as a chopper frequency in this design.

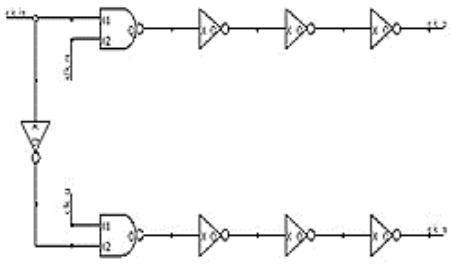

Figure 18 Schematic of clock generator.

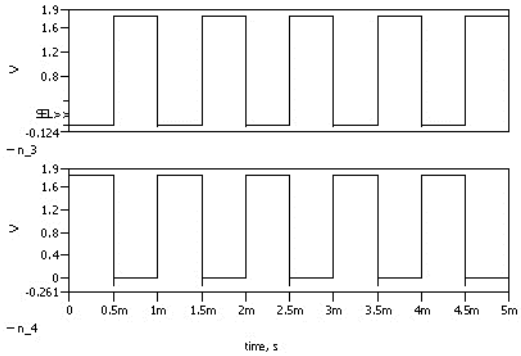

Figure 19 Non-overlap clocks.

Buffer

The buffer is a very important block which is used in the forward path as well as at the output of an amplifier. The single-stage differential amplifier is used as the gain requirement is not high and it needs low output impedance. The basis current requirement for the buffer is 1 μA. The schematic of the buffer is shown in **Figure 20**. In **Figure 21**, the transient analysis is shown as a reference.

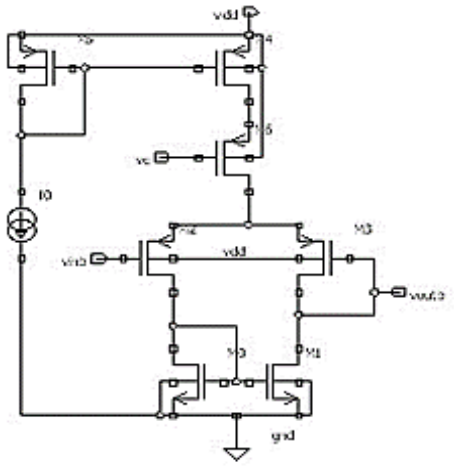

Figure 20 Schematic of buffer.

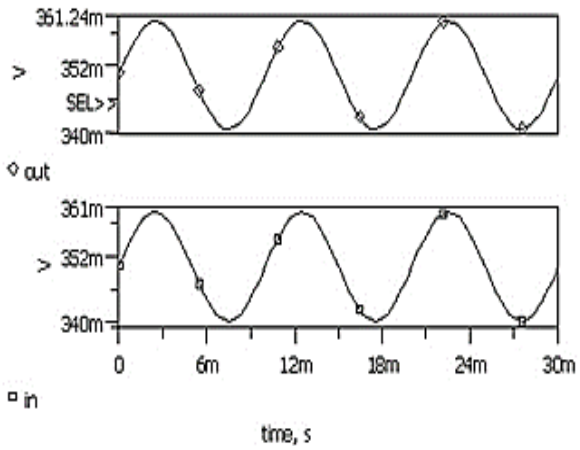

Figure 21 Transient analysis of buffer.

Improvement in input impedance

As in **Figure 22**, to improve the input impedance, a forward path is added in parallel to the input branch to reduce the total charge on capacitors C_{in}. As a result, the input DC and thus the input impedance can be increased. Also, the input impedance is dependent on the chopping frequency. Thus, as per the specification, the balancing between them is very crucial as chopping frequency is also critical to designing OTA to reduce 1/f noise.

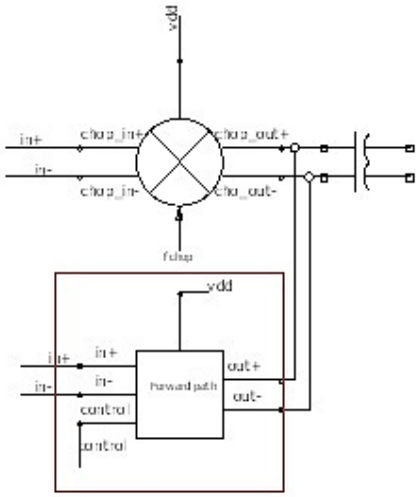

Figure 22 Modification in input branch.

In the forward path,a buffer with a gain of 40dB and a biasing current of 1µA is designed. It adds some power to total power consumption, but this design can further be thought of as a duty-cycled precharge of Cin by controlled buffer so that the additional power can be neglected.

In **Figure 23**, the DC input current is shown with respect to time. In this, it has been observed that at the time of clock transition, some charges occur due to the resultant finite current increases which limit the input impedance, which can be solved by the inclusion of forward-path.The result of DC input current, inclusion after forwarding path, is shown in **Figure 24**.

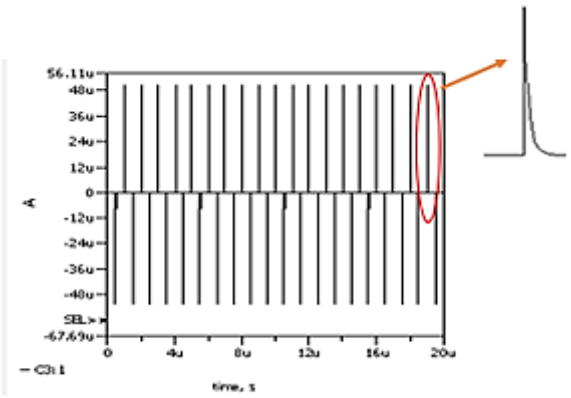

Figure 23 Input current without forwarding path.

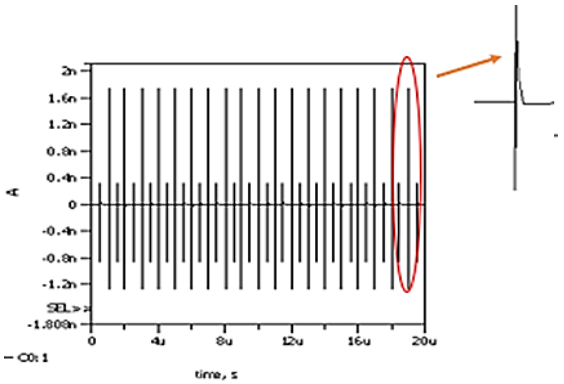

Figure 24 Input current with forwarding path.

Reduction in output ripple

In **Figure 25**, the output branch of the OTA is shown. Here, the R-C network is added at the output of an amplifier to reject the ripples.

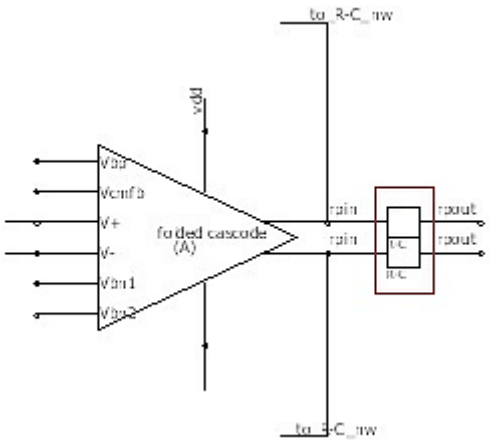

Figure 25 Modification at output branch.

In this design, the offset and the noise are passed through the chopper once only, so that the up-modulation of the offset and noise occurrs due to the ripple generated at the output. In **Figure 26**, the simulation shows the output waveform without the addition of the R-C ripple removing block. The R-C resonant network is tuned in such a way that it is an open circuit at low frequency as its equivalent impedance is higher than the output impedance of the OTA and it is a shot circuit at the chopping frequency so that the desired signal can be passed and ripples due to up-modulated offset and noise can be rejected. In **Figure 27**, the output waveform after the inclusion of the R-C resonant block is shown.

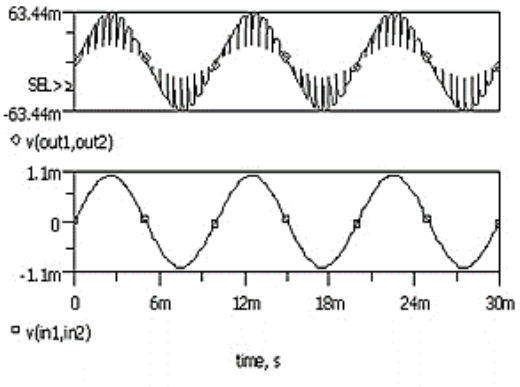

Figure 26 Output without DC block.

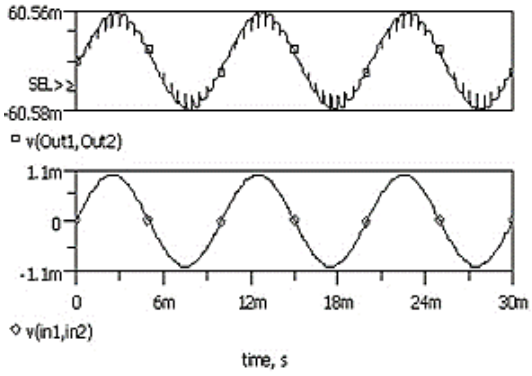

Figure 27 Output with DC block.

Overall result

In **Figure 28**, the periodic AC analysis is shown in which the response is highpass filter with a band of 0.1 to 1kHz. Also, it represents a gain of 100, i.e.,40 dB.

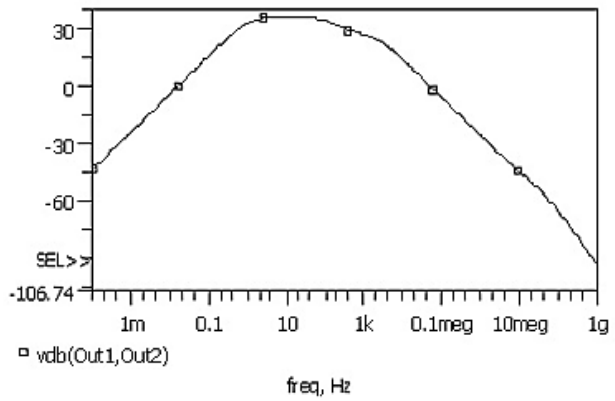

Figure 28 AC analysis of proposed amplifier.

Layout design

The floor plan and layout of the proposed design are shown in **Figures 29** and **30**, respectively, which are designed in the Magic layout tool. The total layout area of the design is 279.8 by 177.1 μm^2.

During the layout preparation, the major challenges are regarding the matching of the differential amplifier and current mirror circuits of the OTA. Also, drawing a layout of passive elements with proper matching is a major issue as it affects CMRR as well. After completing the layout, post-layout simulation was carried out to validate the design.

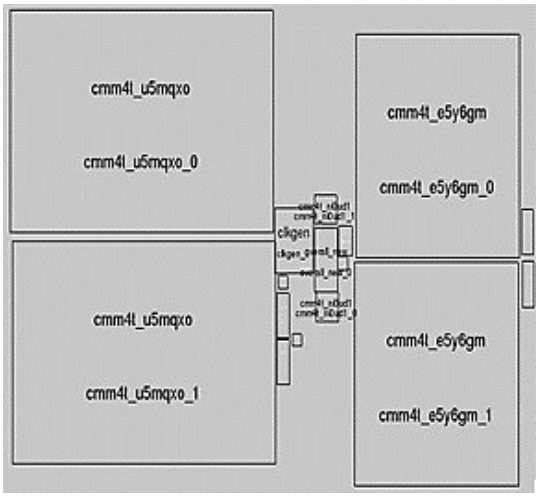

Figure 29 Floorplan of design.

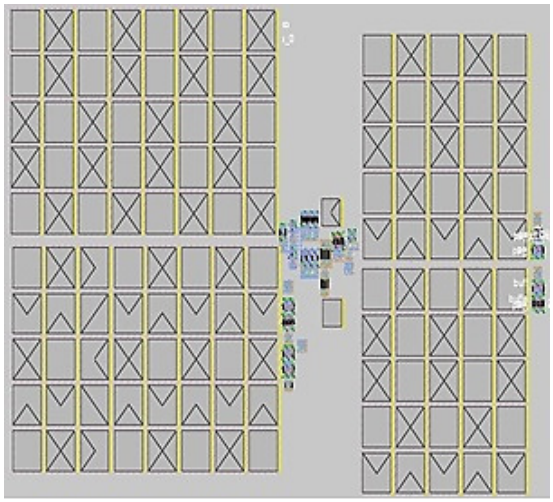

Figure 30 Layout of design.

Comparison analysis

In this section, the comparison analysis with different literature is shown.

Table 1 Comparative analysis.

Parameters	[2]	[6]	[13]	[15]	This work
Process (nm)	180	180	180	180	180
Supply (V)	1.8	1.25	1.8	2.7	1.8
Gain (dB)	34.7	-	30	40	40
Power (μW)	4.2	2.12	75	-	9
Bandwidth (kHz)	0.1	10	1	2	0.1-1
CMRR (dB)	71.5	85	100	51	82
Noise (nV/√Hz)	250	45	75	3.76	42
NEF	-	-	-	2.65	2.2

Conclusions

The proposed biopotential amplifier architecture outperformed the standard chopper amplifier architecture. By including a forward path and an R-C network, the input impedance was increased and the output current ripple was reduced. However, power consumption was increased as a result of the additional buffer in the forward channel, which might be lowered in the future with the installation of a controlled buffer.To ensure lower power dissipation,the design used only 1 OTA with a removed lowpass filter. Besides, the bandpass response of an amplifier helped reduce the offset and flicker (1/f) noise. The design was optimized for a DC gain of 40dB with power dissipation of 9μW and noise of 42 nV/√Hz. Further, the input impedance was boosted (≥200M) and the offset was reduced by 10 μV.

References

[1] CJ Lee and JI Song. A chopper stabilized current-feedback instrumentation amplifier for EEG acquisition applications. *IEEE Access* 2019; **7**, 11565-9.

[2] S Chauhan and LM Saini. Low power and low noise instrumentation amplifier. *In*: Proceedings of the 2nd International Conference on Intelligent Computing and Control Systems, Madurai, India. 2018, p. 1332-5.

[3] H Chandrakumar and D Markovic. A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. *IEEE J. Solid-State Circuits* 2017; **52**, 645-56.

[4] RR Harrison and C Charles. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE J. Solid-State Circuits*2003; **38**,958-65.

[5] H Chandrakumar and D Markovic. A simple area-efficient ripple-rejection technique for chopped biosignal amplifiers. *IEEE Trans. Circuits Syst. II Express Briefs* 2015; **62**, 189-93.

[6] J Wu, MK Law, PI Mak and RP Martins. A 2-μW 45-nV/√Hz readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudofeedback DC servo loop.*IEEE Trans. Circuits Syst. II Express Briefs*2016; **63**, 351-5.

[7] AChandrakasan.*Integrated circuits and systems*. Springer Fachmedien Wiesbaden GmbH, Wiesbaden, Germany, 2014.

[8] Y Agrich, V Lifshits, Y Pavlyuk, I Gureev and D Vorobyev. CMOS amplifier with chopper stabilization and offset calibration. *In*: Proceedings of the IEEE Conference of Russian Young

Researchers in Electrical and Electronic Engineering, St. Petersburg and Moscow, Russia. 2020, p. 2336-9.

[9] A Bagheri, MT Salam, JLP Velazquez and R Genov. Low-frequency noise and offset rejection in dc-coupled neural amplifiers: A review and digitally-assisted design tutorial. *IEEE Trans. Biomed. Circuits Syst*. 2017; **11**, 161-76.

[10] Q Fan, F Sebastiano, JH Huijsing and KAA Makinwa. A 1.8 μ W 60 nV/√ Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes. *IEEE J. Solid-State Circuits* 2011; **46**, 1534-43.

[11] J Xu, RFYazicioglu, B Grundlehner, P Harpe, KAA Makinwa and CV Hoof. A 160 μW 8-channel active electrode system for EEG monitoring.*IEEE Trans. Biomed. Circuits Syst*. 2011; **5**, 555-67.

[12] R Burt and J Zhang. A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path. *In*: Proceedings of the IEEE International Solid-State Circuits Conference, San Francisco, CA, USA. 2006, p. 386-7.

[13] P Bruschi, FD Cesta, AN Longhitano, M Piotto and R Simmarano. A very compact CMOS instrumentation amplifier with nearly rail-to-rail input common-mode range. *In*: Proceedings of the 40th European Solid State Circuits Conference, Venice Lido, Italy.2014, p. 323-6.

[14] GT Ong and PK Chan. A power-aware chopper-stabilized instrumentation amplifier for resistive Wheatstone bridge sensors.*IEEE Trans. Instrum. Meas*. 2014; **63**, 2253-63.

[15] MG Jomehei and S Sheikhaei. A low-power low-noise CMOSbio-potential amplifier for multi-channel neural recording with active DC-rejection andcurrent sharing. *Microelectronics J*. 2019; **83**, 197-211.