WALAILAK JOURNAL
Applied Sciences
http://wjst.wu.ac.th https://doi.org/10.48048/wjst.2021.21451

CMOS Realizable and Highly Cascadable Structures of First-Order All-Pass Filters

Jitender*, Jitendra MOHAN and Bhartendu CHATURVEDI

Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh 201304, India

(*Corresponding author's e-mail: chhabra437@gmail.com)

Received: 23 March 2021, Revised: 24 April 2021, Accepted: 1 May 2021

Abstract

Two novel resistorless structures of a first-order voltage-mode all-pass filter are presented in the paper. Both the structures employ a fully differential second-generation current conveyor (FDCCII) as the primary active element, in addition to an active resistor. A grounded capacitor is the only passive component used in both the structures. In both the structures, CMOS realization of FDCCII is utilized; hence, these structures are CMOS compatible. Some of the other highly demanded features possessed by the presented all-pass structures are: a simple circuit topology, electronic tunability, high input impedance, constraint-free operation in terms of passive component matching, and low sensitivity figures. The theoretical performances under ideal and non-ideal scenarios are presented in detail. Furthermore, the proposed idea is extended to an N^{th}-order voltage-mode all-pass filter and a quadrature oscillator to explore some of the possible applications. PSPICE simulation results verify the theoretical claims of the presented all-pass filters.

Keywords: All-pass filter, Cascadable, First-order, FDCCII, Voltage-mode

Introduction

An all-pass filter (APF) is widely used in various electronics and communication engineering applications. An APF of first-order [1-26] exhibits a constant gain over the entire frequency range, whereas a phase variation of 180° is observed in the delivered output. This phase variation offered by an APF is of great significance in communication systems where the received signals need to pass through an equalizer in order to equalize the phase delays of the received signals. In addition to this, there are some other useful applications of APFs in the electronics domain, such as in the design of band pass filters which support high-Q operation, multiphase oscillators [1,2], etc. Such a diverse range of applications makes an APF an important research prospect. Therefore, many researchers have contributed towards the design aspects of APFs in the last few decades. One of the most popular structures of APFs is the voltage-mode all-pass filter structure. When it comes to the selection of active building block (ABB) in the designing of any signal processing circuit, there are various contenders, such as buffered amplifiers [1], operational transresistance amplifiers [2], current conveyors [3-25], etc. In the last few decades, current conveyors and their variants as ABBs have been used quite prominently in voltage-mode [1-25] and in current-mode [26] filter designs on account of their inherent benefits, such as simple design structure, high gain-bandwidth product, good CMRR, and support for higher signal bandwidth [13]. Some of the most relevant existing voltage-mode all-pass filter structures [1-25] based on the mentioned ABBs are reviewed here on the basis of performance metrics as listed in **Table 1**.

Table 1 Some relevant performance metrices for a voltage-mode analog signal processing circuit.

Attributes	**Performance metrices**
Design simplicity	Use of single active element, minimal usage of passive components, no component matching condition.
IC realization suitability	Use of grounded passive components.
Support for cascadability	High input impedance and low output impedance.
Acceptable sensitivity figures	Sensitivity figures to be ≤ 1 in magnitude.
Tunability	Either by using device transconductance or by replacing passive resistor(s) with MOS-based active resistor(s).

- Filter realizations based on single active element offer simpler circuit designs in comparison with realizations with more than 1 active element. Circuits of [3,9,14,17-19,21,23] employ 2 active elements.
- In comparison to MOS transistors, passive components like resistors and capacitors take more space during fabrication, thus, their usage should be minimized. Filter structures of [1,2,4-6,8-9,13,14,16,17,19,22] use 3 or more number of passive components.
- Floating passive capacitors are hard to fabricate in comparison to grounded ones. Voltage-mode all-pass filters of [1,2,4,7,8,15,17,22,24] use 1 or more floating capacitors.
- Component matching condition is an additional constraint that needs to be fulfilled to achieve desired filter behavior. This constraint exists in designs of [1,2,4-6,8,9,13,14,16,17,19].
- A voltage-mode circuit should have high input impedance and low output impedance to support the feature of full cascadability. Circuits of [3,10,12-13,15,18-19,23] have this feature.
- In a filter configuration, if a passive resistor is replaced by an active one (in the form of a MOS transistor), a tunable frequency response can be achieved by varying the gate control voltage of the MOS transistor. However, this provision of tunability does not support circuits which require resistor matching constraints [1,2,4-6,8,9,13,14,16,17,19,22], since varying the resistor value may disturb the matching condition. The possibility of incorporating active resistor(s) in place of passive ones is available in the designs of [3,7,10-12,15,18,20,21,23-25], but this aspect is explored in the designs of [11,12,20,21,24,25] only.
- Sensitivity of filter pole frequency with respect to employed resistors, capacitors, and non-ideal transfer gains is another important factor. All the reviewed works [1-25] have sensitivity figures in an acceptable range, i.e., ≤ 1 in magnitude.

Hence, with the perspective of maximizing the availability of these desirable features, 2 voltage-mode all-pass filter structures are proposed. Both the configurations use a single active device, namely FDCCII, 1 grounded capacitor, and an NMOS transistor as an active resistor. Comparison of the proposed filter structures with the reviewed works [1-25] is shown in **Table 2**. Specifically, by observing the proposed works' performance with respect to the works based on FDCCII [10-13,25], it can be seen that the proposed structures employ the least number of MOS transistors for circuit implementation as compared to the structures reported in [10-13,25]. Also, the structure reported in [13] employs 2 resistors and needs component matching constraint to be satisfied.

Materials and methods

This section of the paper describes the mathematical details of the proposed APFs. To start with, basic details of the employed ABB, i.e., FDCCII, are described. Thereafter, the structures of the proposed APFs are described, along with their non-ideal and parasitic study.

Table 2 Comparison of the proposed filter structures with the reviewed works.

Ref	ABB	No. of ABBs	No. of MOS transistors	No. of R	No. of C	All grounded capacitor(s)	Input impedance	Free from matching condition	Power supply (V)	Power consumption (mW)	Pole frequency (MHz)
[1]	CDBA	1	20	2/3/3	2/2/1	No	NA	No	±2.5	NA	1.59
[2]	OTRA	1	20	3	1	No	NA	No	±2.5	NA	0.159
[3]	DVCC	2	24	1	1	Yes	High	Yes	±1.5	0.3	0.636
[4]	CCII+	1	NA	2	1	No	NA	No	±12	NA	0.159
[5]	DO-CCII	1	23	2	1	Yes	High	No	±1.5	NA	1
[6]	MCCII-	1	21	2	1	Yes	High	No	±2.5	NA	1
[7]	DDCC	1	36	1	1	No	NA	Yes	±2.5	NA	1.59
[8]	CCII-	1	NA	2	1	No	NA	No	NA	NA	0.001
[9]	DVCC	2	36	2/1	1/2	Yes	High	No	±2.5	NA	1.5
[10]	FDCCII	1	36	1	1	Yes	High	Yes	±3	NA	3.18
[11]	FDCCII	1	44	1	1	Yes	High	Yes	±1.3	NA	NA
[12]	FDCCII	1	28	1	1	Yes	High	Yes	±1.3	NA	3.18
[13]	FDCCII	1	36	2	1	Yes	High	No	±3.3	NA	1.59
[14]	CCII	2	NA	3	1	Yes	High	No	NA	NA	NA
[15]	DXCCII	1	28	1	1	No	High	Yes	±2.5	NA	25
[16]	CCII-	1	5	3	1	Yes	NA	No	±0.75	0.83	1.59
[17]	DPDVCC	2	92	2	2	No	NA	No	±2.5	NA	0.267
[18]	DVCC	2	24	1	1	Yes	High	Yes	±1.25	1.32	1.59
[19]	DDCC+	1	12	3	1	Yes	NA	No	±1.25	NA	0.0159
	DDCC+	2	24	3	1	Yes	High	No	±1.25	NA	1.59
[20]	DV-DXCCII	1	34 + 1	0*	1	Yes	NA	Yes	±0.9	NA	27
[21]	DDCC-	1	18 + 2	0*	1	No	No	Yes	±1.5	NA	0.159
	DDCC- and DDCC+	1 + 1	32 + 2	0*	1	Yes	High	Yes	±1.5	NA	0.159
[22]	DVCC	1	12	1/2	2/1	No	NA	No	±2.5	NA	0.395
[23]	DDCC	2	20	1	1	Yes	High	Yes	±2.5	4.9	1.59
[24]	DD-DXCCII	1	38 + 1	0*	1	No	NA	Yes	±1.25	NA	6
[25]	FDCCII	1	44	1	1	Yes	NA	Yes	±3	NA	0.159
Proposed voltage-mode all-pass filter-I	**FDCCII**	**1**	26 + 1	0*	1	**Yes**	**High**	Yes	±1.25	2	6.37
Proposed voltage-mode all-pass filter-II	**FDCCII**	**1**	26 + 1	0*	1	**Yes**	**High**	Yes	±1.25	2	6.37

Abbreviations: CDBA: Current differencing buffered amplifier, OTRA: Operational trans-resistance amplifier, DVCC: Differential voltage current conveyor, CCII+: Positive type second-generation current conveyor, DO-CCII: Dual-output second generation current conveyor, MCCII-: Modified negative type second-generation current conveyor, DDCC: Differential difference current conveyor, DDCC-: Inverting differential difference current conveyor, DDCC+: Non-inverting differential difference current conveyor. CCII-: Negative type second-generation current conveyor, FDCCII: Fully differential second generation current conveyor. CCII: Second-generation current conveyor, DXCCII: Dual-X second-generation current conveyor, DPDVCC: Digitally programmable differential voltage current conveyor, DV-DXCCII: Differential voltage dual-X second-generation current conveyor, DD-DXCCII: Differential difference dual-X second-generation current conveyor, ABB: Active building block, MOS: Metal oxide semiconductor, R: Resistor, C: Capacitor, NA: Not available, *: Resistorless realization is presented.

Description of ABB: FDCCII

FDCCII [27] was introduced in 2000 and is an extension of a CCII structure in a way to exploit the benefits of fully differential signal processing with an additional benefit of enhancement of dynamic range. It has featured in some important signal processing applications, such as filters and oscillators [28]. Usually, it is an eight-port device, but the proposed filter applications do not require the Z_n stage; therefore, it is eliminated from the structure presented in [29]. Its symbolic representation is presented in **Figure 1**. The relations existing between the various FDCCII ports are represented in matrix form as follows.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{Xp} \end{bmatrix} \quad (1)$$

The CMOS implementation is also presented in **Figure 2**, which comprises of 26 interconnected MOS transistors (after eliminating the Z_n stage). The fully differential voltages applied at high impedance Y-terminals are conveyed to the low impedance X-terminals, and the current I_{Xp} from X_p terminal is conveyed to high impedance Z_p terminals as I_{Zp}.

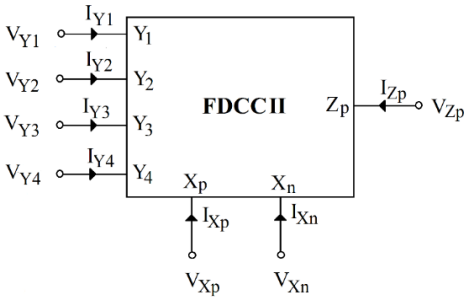


Figure 1 Symbolic representation of FDCCII.

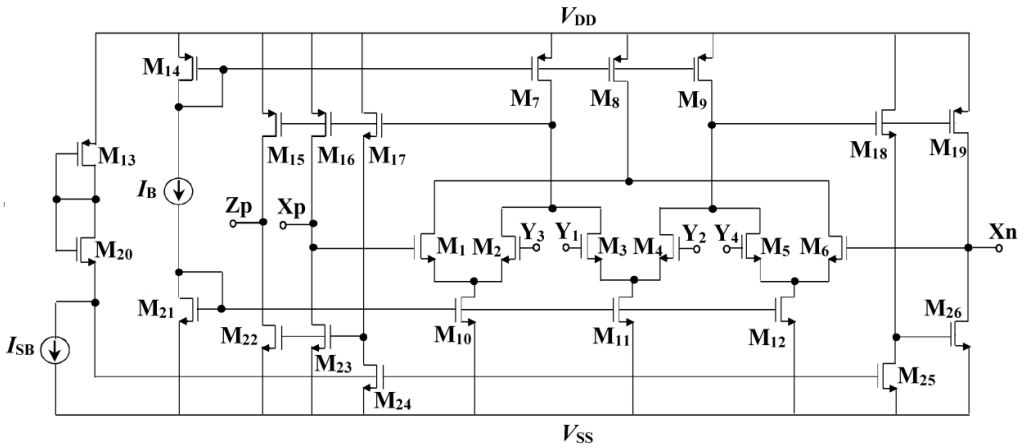


Figure 2 CMOS implementation of FDCCII [29].

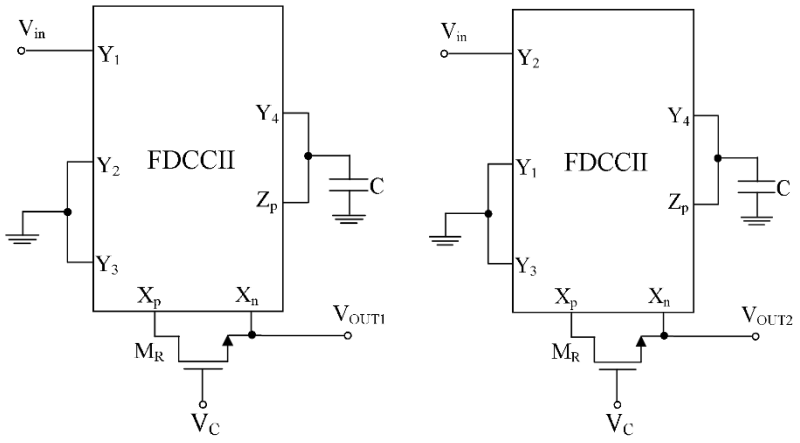


Figure 3 Proposed first-order circuit structures (a) voltage-mode all-pass filter-I, (b) voltage-mode all-pass filter-II.

Proposed All-Pass Circuits

Each of the proposed first-order voltage-mode all-pass filter configurations offer a simple design topology and consist of a single FDCCII, a single grounded capacitor, and an NMOS transistor as an active resistor. The presence of the active resistor imparts tunability to the design [11-12,20-21,24-25]. Structures of the proposed configurations are depicted in **Figure 3**. It is to be noted from **Figure 3** that input is applied at the high impedance terminal and output is available from the low impedance terminal. Proposed voltage-mode all-pass filter circuits are analyzed using port relation matrix, as expressed in Eq. (1), and their corresponding nodal equations. The obtained transfer functions are expressed in Eqs. (2) and (3).

$$\frac{V_{OUT1}}{V_{in}} = -\left(\frac{sR_M C - 1}{sR_M C + 1}\right) \tag{2}$$

$$\frac{V_{OUT2}}{V_{in}} = \left(\frac{sR_M C - 1}{sR_M C + 1}\right) \tag{3}$$

Here, R_M is the resistance of the externally connected NMOS transistor M_R, and is expressed as:

$$R_M = \left[\mu_n C_{ox}\left(\frac{W}{L}\right)(V_C - V_t)\right]^{-1} \tag{4}$$

where C_{ox}: capacitance of oxide layer, μ_n: mobility of electrons over the surface of the semiconductor, V_C: gate control voltage, W/L: aspect ratio of transistor M_R, and V_t: threshold voltage.

The pole frequency expression is identical for both of the proposed voltage-mode all-pass filter structures and is expressed in Eq. (5).

$$\omega_0 = \frac{1}{R_M C} \tag{5}$$

Phase angle expressions, as observed from Eqs. (2) and (3), are given as follows.

$$\phi_{OUT1} = -2\tan^{-1}(\omega R_M C) \tag{6}$$

$$\phi_{OUT2} = 180^o - 2\tan^{-1}(\omega R_M C) \tag{7}$$

It is also observed from Eqs. (2) to (5) that voltage-mode all-pass filter-I is an inverting one and voltage-mode all-pass filter-II is a non-inverting one.

Proposed circuits are analyzed for sensitivity performance, and good sensitivity figures (equal to unity in magnitude) are observed, as can be seen from Eq. (10).

$$S_C^{\omega_0} = S_{R_M}^{\omega_0} = -1 \tag{8}$$

A noteworthy observation from the circuit analysis is the absence of any component matching condition, which helps to achieve the desired responses in a constraint free manner.

FDCCII's Non-Ideal Behavior

Considering the fact that an active device always deviates from its expected behavior to some extent when some passive components are connected to form a circuit, therefore, it becomes important to study the effects of non-idealities on the circuit's runtime performance. To understand the effects of non-idealities on the behavior of the proposed filter configurations, non-ideal port relations, as summarized in Eq. (9), are used while performing the circuit analysis.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ -\beta_4 & \beta_5 & 0 & \beta_6 & 0 \\ 0 & 0 & 0 & 0 & \alpha_1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{Xp} \end{bmatrix} \tag{9}$$

Here, $\beta_{i\ (i=\ 1\ to\ 6)}$ and α_1 are non-ideal voltage transfer gains and a non-ideal current transfer gain, respectively. Transfer functions thus obtained after using above mentioned non-ideal port relations are shown in Eqs. (10) and (11).

$$\frac{V_{OUT1}}{V_{IN}} = -\frac{sR_M C\beta_4 - \alpha_1\beta_1\beta_6}{sR_M C + \alpha_1\beta_6} \tag{10}$$

$$\frac{V_{OUT2}}{V_{IN}} = \frac{sR_M C\beta_5 - \alpha_1\beta_2\beta_6}{sR_M C + \alpha_1\beta_6} \tag{11}$$

The pole frequency expression for the non-ideal scenario, as observed from Eqs. (10) and (11), is expressed as follows.

$$\omega_0 = \frac{\alpha_1\beta_6}{R_M C} \tag{12}$$

Sensitivity figures for pole frequency of the proposed filters are given below.

$$S_C^{\omega_0} = S_{R_M}^{\omega_0} = -1 \tag{13}$$

$$S_{\beta_6}^{\omega_0} = S_{\alpha_1}^{\omega_0} = 1 \tag{14}$$

All active and passive sensitivity figures have unity magnitude; thus, the proposed all-pass filters show promising performance in the non-ideal scenario as well.

Parasitic Study

The parasitic qualities of FDCCII are further studied to analyze their impact on the performance of the proposed voltage-mode all-pass filters. The parasitic model of FDCCII is presented in **Figure 4**. Z_{Y1}, Z_{Y2}, Z_{Y3}, and Z_{Y4} are the parasitic impedances associated with the input terminals Y_1, Y_2, Y_3, and Y_4, respectively. Z_{Zp} is the parasitic impedance associated with output terminals Z_p. All impedances are composites of parasitic resistance and capacitance connected in shunt with the associated ports. R_{Xp} and R_{Xn} are series parasitic resistances associated with the low impedance terminals X_p and X_n. Effect of parasitic on voltage-mode all-pass filter-I is studied using the parasitic model as shown in **Figure 4**. All-pass response is directly available at X_n terminal, thereby eliminating the impact of small parasitic resistances. Y_2 and Y_3 terminals are grounded, and input is applied across the Y_1 terminal, which goes well with the parasitic compensation point of view. Therefore, the performance of the proposed filters is less affected.

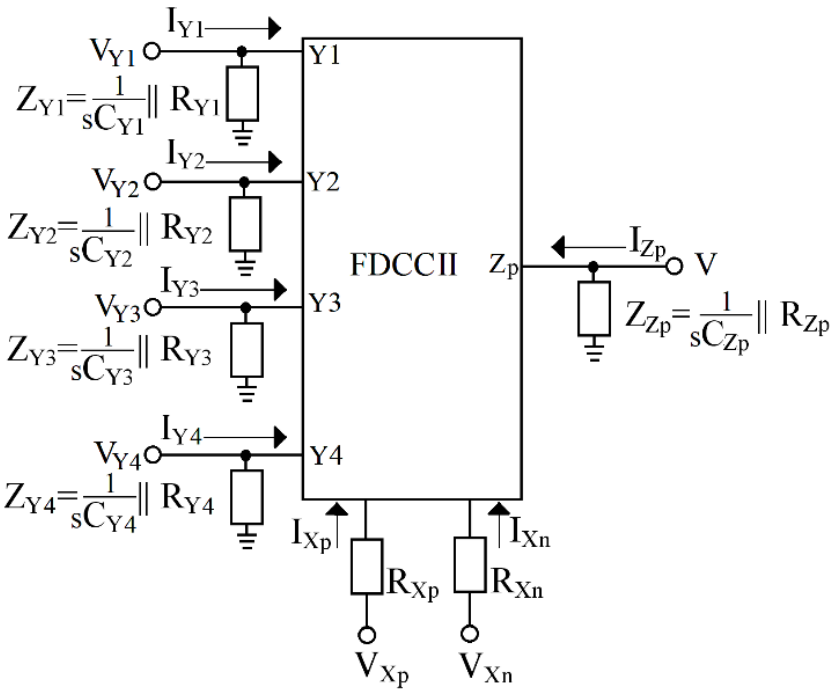


Figure 4 Parasitic model of FDCCII.

Updated transfer functions obtained after taking the parasitic impedances into account are expressed as:

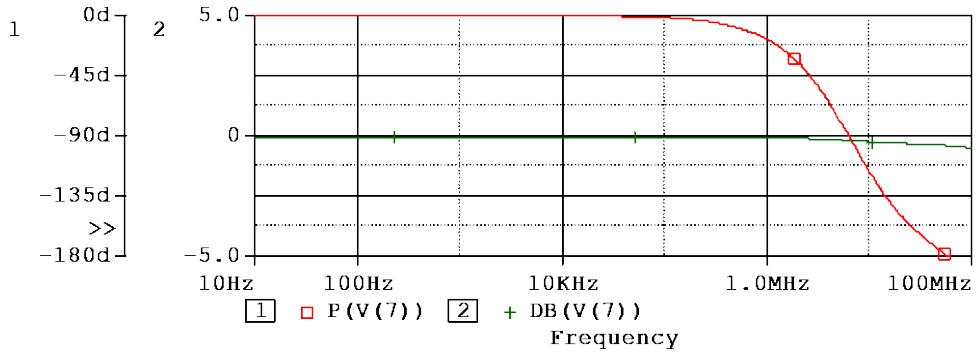
$$\frac{V_{OUT1}}{V_{in}} = -\left(\frac{R'' - R_{Xn}}{R'' + R_{Xn}}\right)\left(\frac{s - \dfrac{R_{Xn} + R' - R''}{R'(R'' - R_{Xn})(C + C_P)}}{s + \dfrac{R_{Xn} + R' + R''}{R'(R'' + R_{Xn})(C + C_P)}}\right) \tag{15}$$

$$\frac{V_{OUT2}}{V_{in}} = \left(\frac{R'' - R_{Xn}}{R'' + R_{Xn}}\right)\left(\frac{s - \dfrac{R_{Xn} + R' - R''}{R'(R'' - R_{Xn})(C + C_P)}}{s + \dfrac{R_{Xn} + R' + R''}{R'(R'' + R_{Xn})(C + C_P)}}\right) \tag{16}$$

Here, $R' = R_{Zp} \| R_{Y4}$, $R'' = R_{Xp} + R_M$, and $C_P = C_{Zp} + C_{Y4}$.

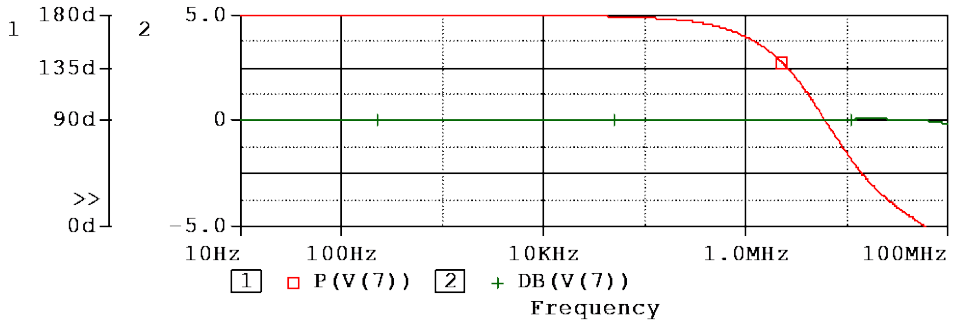
Results and discussion

PSPICE simulations using 180 nm CMOS technology parameters [30] are done to validate the operations of proposed voltage-mode all-pass filter-I and voltage-mode all-pass filter-II. Supply voltages V_{DD} and V_{SS} are chosen to be ±1.25 V. Bias currents I_B and I_{SB} are 65 and 50 µA, respectively. Capacitor value is chosen to be 5 pF. For externally connected NMOS transistor, W/L ratio is 1.46/0.72 µm and applied control voltage is 0.8 V. This results in an effective resistance of 5 kΩ. For all NMOS and PMOS transistors used in CMOS implementation of FDCCII [29], W/L ratios are 3.6/0.72 µm and 7.2/0.72 µm, respectively. Combined gain and phase plots for the proposed voltage-mode all-pass filter-I and voltage-mode all-pass filter-II are shown in **Figures 5(a)** and **5(b)**, respectively. Phase variations of 0° to –180° and 180° to 0° for voltage-mode all-pass filter-I and voltage-mode all-pass filter-II, respectively, are clearly observed from **Figure 5**. Further, ideal and simulated phase and gain responses of the proposed filters are additionally plotted in **Figure 5(c)** to justify the run-time performance of the proposed filters.



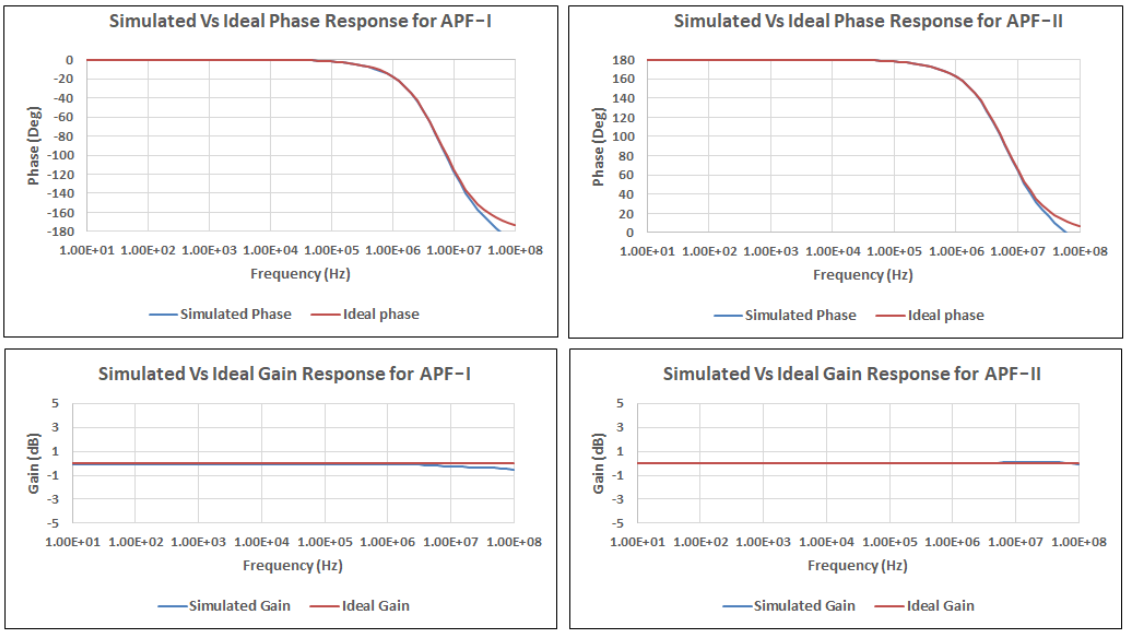
□ : Phase (Deg) + : Gain (dB)

(a)



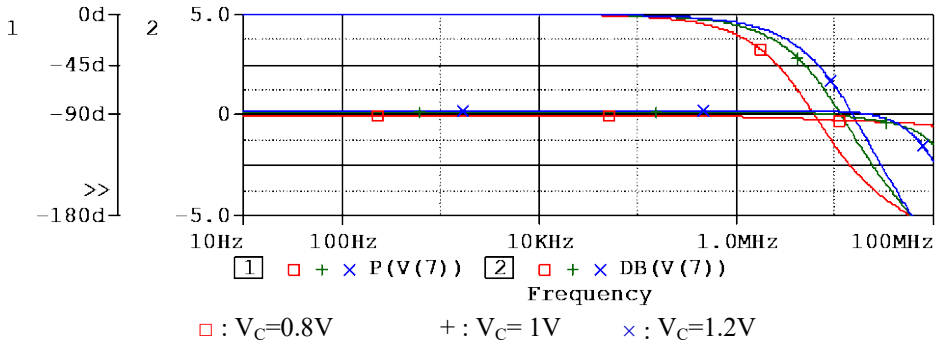
□ : Phase (Deg) + : Gain (dB)

(b)



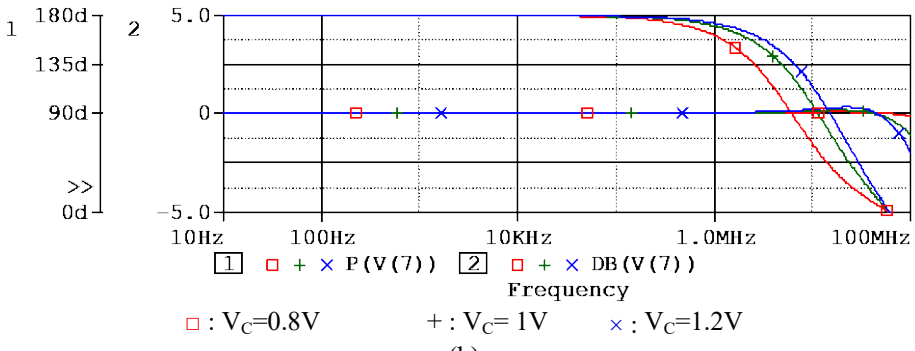
(c)

Figure 5 (a) Gain and phase plots for voltage-mode all-pass filter-I, (b) Gain and phase plots for voltage-mode all-pass filter-II, and (c) Simulated vs ideal gain and phase plots for all-pass filter-I and all-pass filter-II.



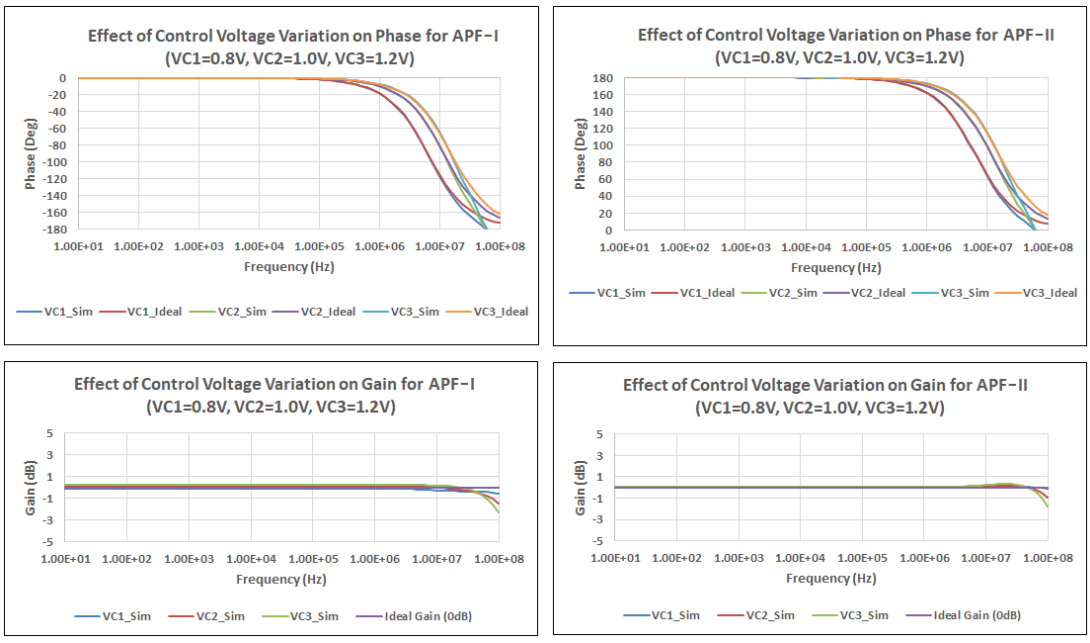
□ : V_C=0.8V + : V_C= 1V × : V_C=1.2V

(a)



□ : V_C=0.8V + : V_C= 1V × : V_C=1.2V

(b)

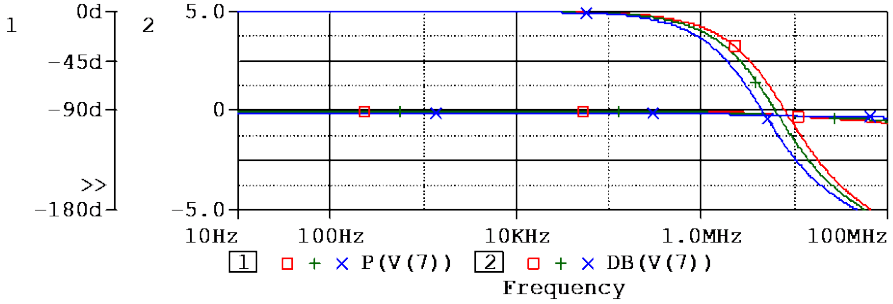


(c)

Figure 6 (a) Variation in gain and phase plots with gate control voltage for voltage-mode all-pass filter-I, (b) Variation in gain and phase plots with gate control voltage for voltage-mode all-pass filter-II, and (c) Simulated vs ideal gain and phase plots with variation in gate control voltage for all-pass filter-I and all-pass filter-II.

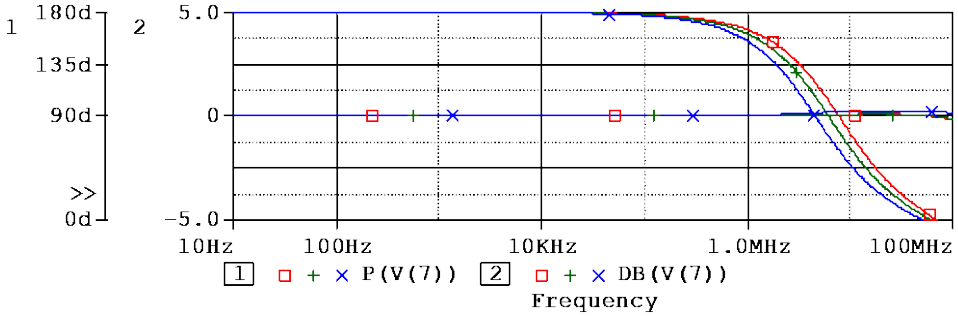
Pole frequency of the proposed voltage-mode all-pass filters can be easily tuned by varying the external gate control voltage V_C, as depicted in **Figure 6**. Effects of device non-idealities and parasitic qualities can be observed as deviations between the simulated and ideal responses, depicted in **Figures 5(c)** and **6(c)**. AC response of the proposed voltage-mode all-pass filters under varying temperature conditions (–25 to 100 °C) is also shown in **Figure 7**, which shows that gain is almost unaffected by temperature variations, but the phase changes are significant. Simulated pole frequency for voltage-mode all-pass filter-I and voltage-mode all-pass filter-II is 6.36 MHz. At this pole frequency, time domain waveforms of input and output voltages and their corresponding Lissajous patterns for voltage-mode all-pass filter-I and voltage-mode all-pass filter-II are depicted in **Figures 8** and **9**, respectively. In **Figure 8(a)** the output voltage leads the input voltage by 90°, whereas in **Figure 9(a)**, the output voltage lags behind the input voltage by 90°. The phase changes depicted in **Figures 8(a)** and **9(a)** are in accordance with the characteristics of first-order inverting and non-inverting all-pass filters, respectively, which cause a 90° phase shift in output signal at the pole frequency. The signal selectivity around the pole frequency is evident from the frequency spectrums depicted in **Figure 10**. Power dissipated by both voltage-mode all-pass filters is 2 mW.

Behavior of the voltage-mode all-pass filters for variation in capacitor values is also observed by performing Monte-Carlo (MC) analysis. For 100 runs and 10 % Gaussian deviation in capacitor value, MC simulation results for pole frequency of voltage-mode all-pass filter-I and voltage-mode all-pass filter-II are shown in **Figure 11**. MC histograms clearly show that the effects of variation in capacitor values have minimal effect on the performances of the proposed voltage-mode all-pass filter structures. Furthermore, an N^{th}-order APF and a quadrature oscillator are presented as the application of the proposed voltage-mode all-pass filter-I.



□ : Temp = –20 °C + : Temp = 0 °C × : Temp = 100 °C

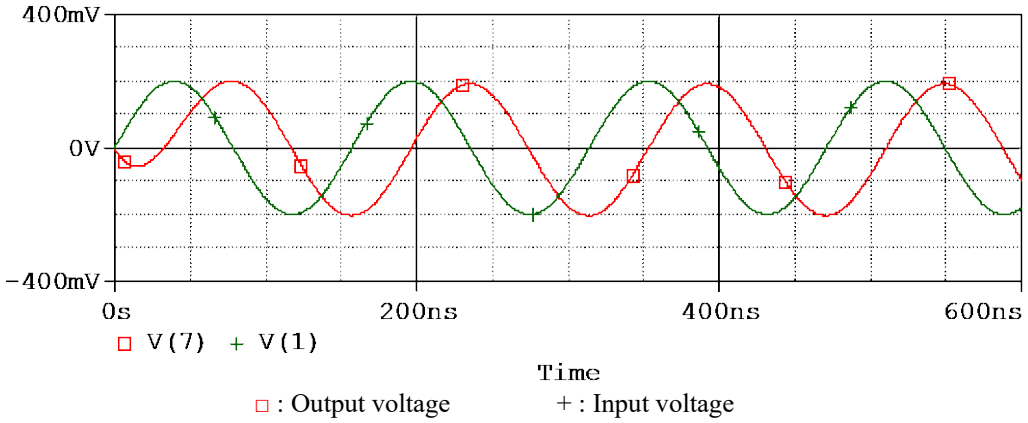
(a)



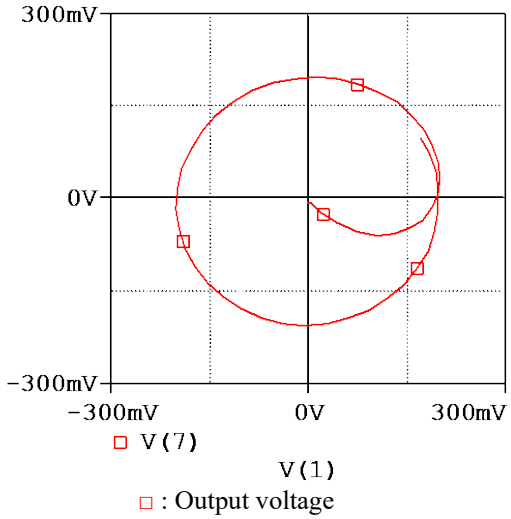
□ : Temp = –20 °C + : Temp = 0 °C × : Temp = 100 °C

(b)

Figure 7 Gain and phase responses for varying temperatures for (a) voltage-mode all-pass filter-I and (b) voltage-mode all-pass filter-II.

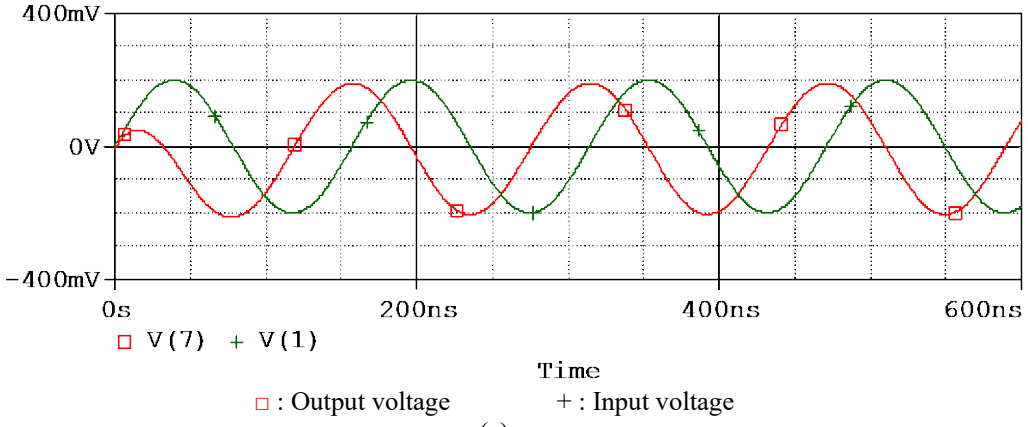


(a)

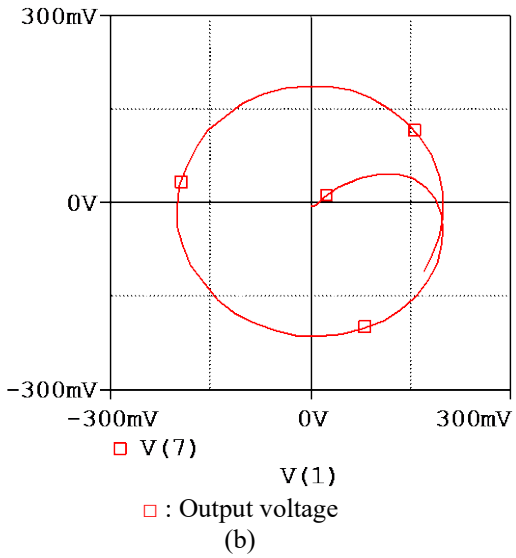


(b)

Figure 8 Voltage-mode all-pass filter-I (a) transient response and (b) Lissajous pattern.

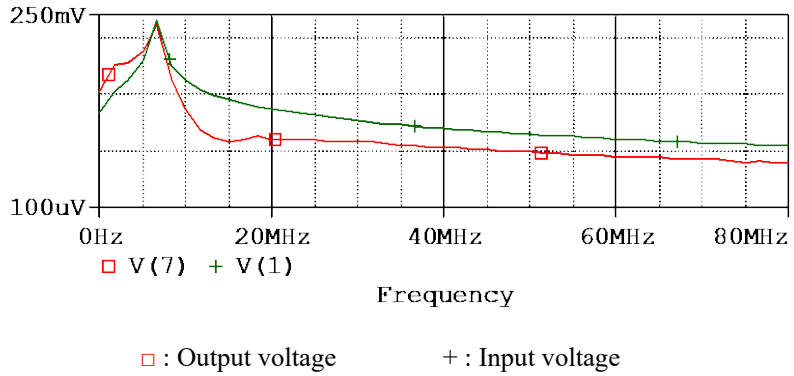


(a)

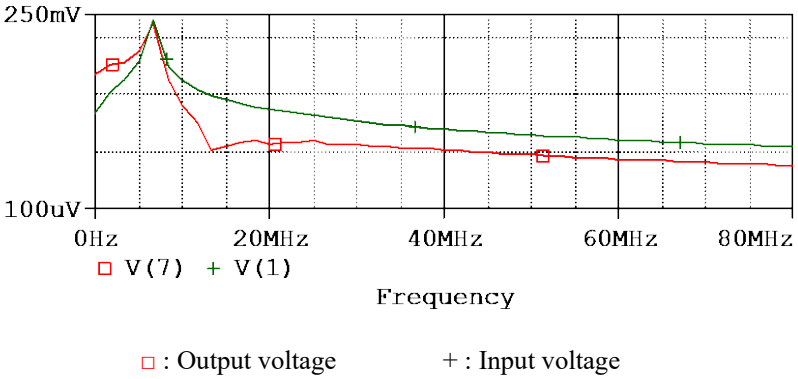


(b)

Figure 9 Voltage-mode all-pass filter-II (a) transient response and (b) Lissajous pattern.

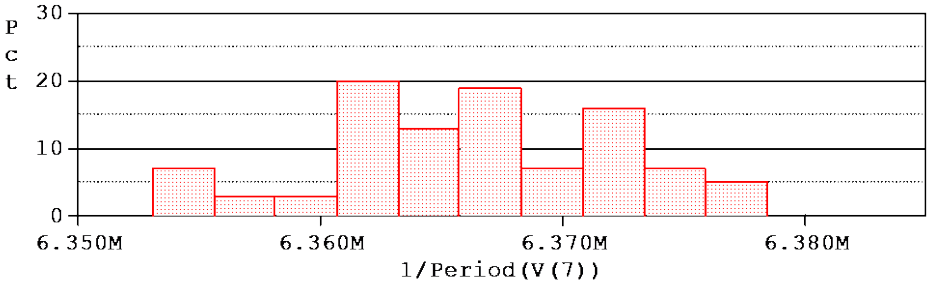


(a)



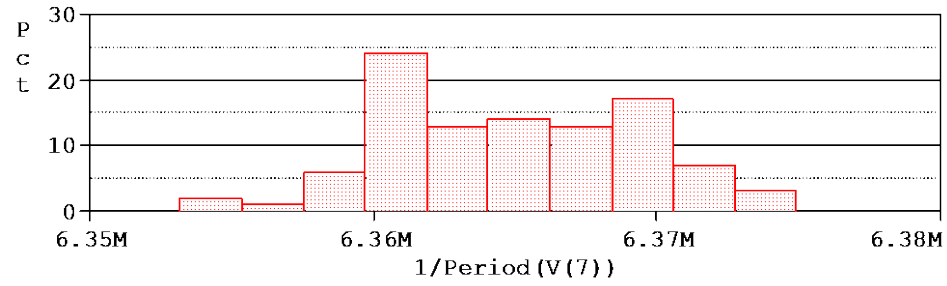
(b)

Figure 10 Frequency spectrums at pole frequency for (a) voltage-mode all-pass filter-I and (b) voltage-mode all-pass filter-II.



n samples	= 100	10th %ile	= 6.35828e+006
n divisions	= 10	median	= 6.36708e+006
mean	= 6.36638e+006	90th %ile	= 6.37537e+006
sigma	= 6153.93	maximum	= 6.37845e+006
minimum	= 6.35307e+006	3*sigma	= 18461.8

(a)



n samples	= 100	10th %ile	= 6.35995e+006
n divisions	= 10	median	= 6.36431e+006
mean	= 6.36479e+006	90th %ile	= 6.37042e+006
sigma	= 4527.19	maximum	= 6.37492e+006
minimum	= 6.3532e+006	3*sigma	= 13581.6

(b)

Figure 11 MC histograms with 10 % capacitor variations for (a) voltage-mode all-pass filter-I and (b) voltage-mode all-pass filter-II.

Application as Nth-Order All-Pass Filter

As mentioned in earlier sections, the proposed voltage-mode all-pass filters support the feature of cascadability. To demonstrate the feature of cascadability, the proposed structure of voltage-mode all-pass filter-I is extended to form an Nth-order all-pass filter in this section. The circuit of the proposed Nth-order voltage-mode all-pass filter is shown in **Figure 12**.

Transfer function obtained for Nth-order voltage-mode all-pass filter is expressed as:

$$\frac{V_{OUT(N)}}{V_{IN}} = \left(\frac{1-sR_{M1}C_1}{1+sR_{M1}C_1}\right)\times\left(\frac{1-sR_{M2}C_2}{1+sR_{M2}C_2}\right)\times....\times\left(\frac{1-sR_{MN}C_N}{1+sR_{MN}C_N}\right) \quad (17)$$

Pole frequency expression, as observed from Eq. (17), is given below.

$$\omega_0 = \left(\frac{1}{R_{M1}C_1} \times \frac{1}{R_{M2}C_2} \times \ldots \times \frac{1}{R_{MN}C_N} \right)^{1/N} \tag{18}$$

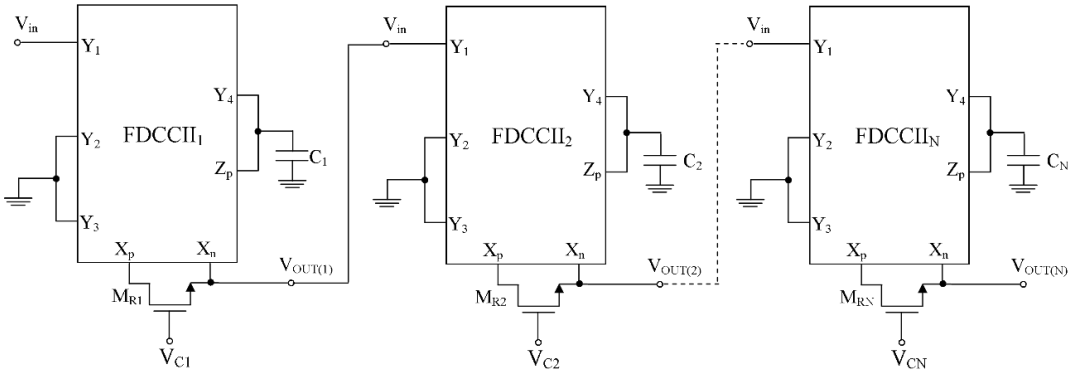


Figure 12 An N[th]-order voltage-mode all-pass filter extended from voltage-mode all-pass filter-I.

Using Eq. (18), for N = 2, i.e., a second-order voltage-mode all-pass filter, pole frequency expression can be expressed as:

$$\omega_0 = \left(\frac{1}{R_{M1}C_1R_{M2}C_2} \right)^{1/2} \tag{19}$$

PSPICE simulations for second-order voltage-mode all-pass filter circuit are also carried out using the same values of supply voltages and bias currents as used for voltage-mode all-pass filter-I. Values of both the capacitors, i.e., C_1 and C_2, are chosen to be 5 pF. Gate control voltages V_{C1} and V_{C2} are chosen as 0.8 V to realize resistors of 5 kΩ. A plot showing AC response of second order voltage-mode all-pass filter is depicted in **Figure 13**. Phase variation of 360° in output voltage is clearly observed from the phase response. Pole frequency thus obtained from simulation results is 6.36 MHz. Transient response at pole frequency value is shown in **Figure 14**, which shows a 180° phase shift between the input and output voltages.

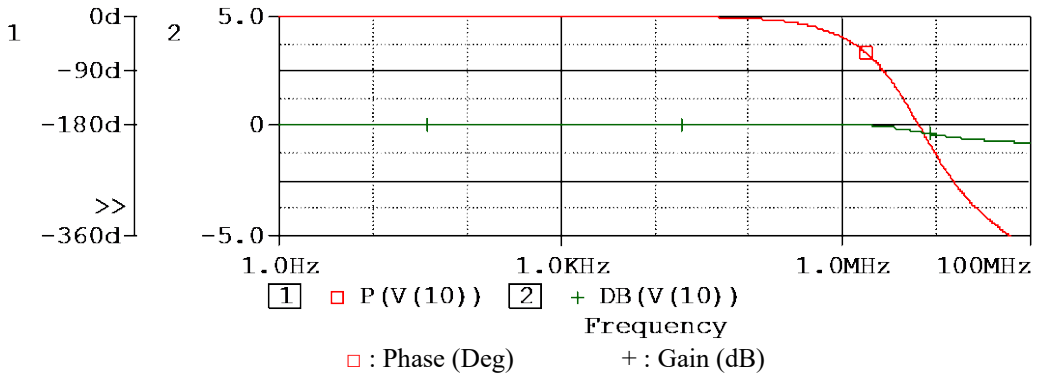


Figure 13 Gain and phase plot for second-order voltage-mode all-pass filter.

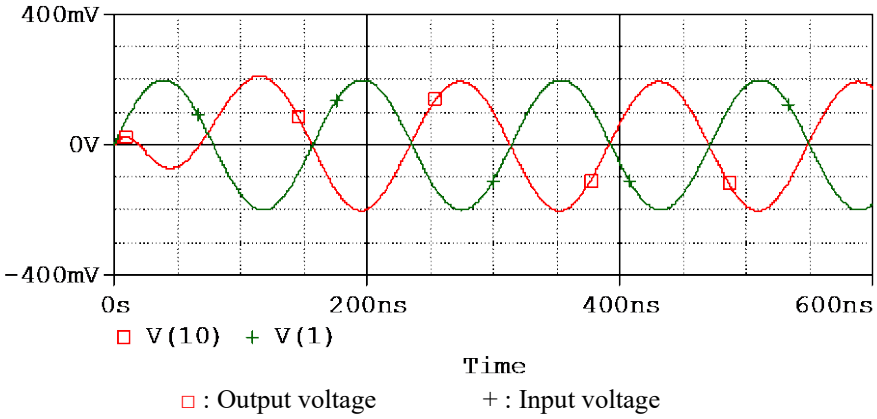


Figure 14 Transient response for 2nd order voltage-mode all-pass filter.

Application as Quadrature Oscillator

An all-pass filter can be used to design multi-phase oscillators by various methods. One such frequently employed method is to connect an all-pass filter and an integrator in a closed loop [31]. Doing so, the designed circuit yields the characteristic equation of an oscillator. The same concept is employed here to design a quadrature oscillator from the circuit of the proposed voltage-mode all-pass filter-I. The derived oscillator circuit is shown in **Figure 15**.

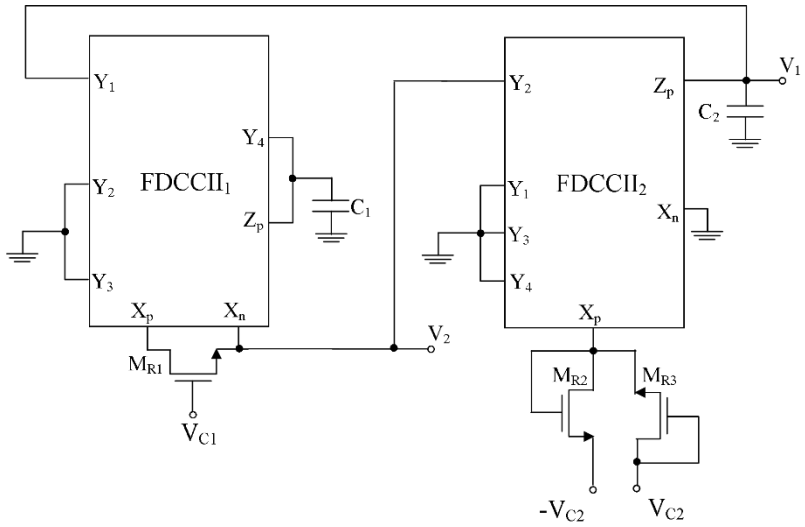


Figure 15 Quadrature oscillator derived from proposed voltage-mode all-pass filter-I.

On multiplying the transfer functions of the proposed voltage-mode all-pass filter-I and FDCCII-based integrator and equating the resultant product to unity, the characteristic equation of the derived oscillator is expressed as:

$$s^2 R_{M1} R_{M2} C_1 C_2 + s(R_{M2} C_2 - R_{M1} C_1) + 1 = 0 \quad (20)$$

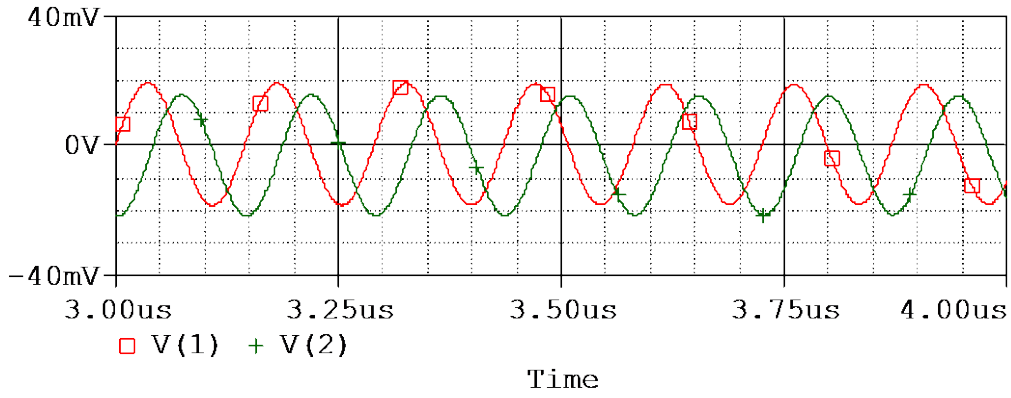
Here, R_{M1} is the resistance offered by transistor M_{R1} which is acting as a floating resistor [31], and R_{M2} is the active replacement of grounded resistor formed by the combination of transistors M_{R2} and M_{R3} [32].

Observing Equation 20 yields the condition of oscillation and frequency of oscillation (FO), as expressed in Eqs. (21) and (22).

$$R_{M2}C_2 \leq R_{M1}C_1 \tag{21}$$

$$\omega_0 = \left(\frac{1}{R_{M1}R_{M2}C_1C_2}\right)^{\frac{1}{2}} \tag{22}$$

The derived oscillator circuit is also simulated on PSPICE using 180 nm CMOS parameters [30]. Values of both the capacitors are chosen to be 5 pF, whereas gate control voltages V_{C1} and V_{C2} are chosen as 0.8 V to realize resistors of 5 kΩ. Simulated value of FO is found to be 6.34 MHz, which is quite close to the theoretical value of 6.37 MHz. Quadrature output voltages V_1 and V_2 obtained from oscillator are depicted in **Figure 16**.



□ : Voltage output V_1 + : Voltage output V_2

Figure 16 Quadrature output voltages V_1 and V_2 obtained from derived quadrature oscillator.

Conclusions

Two novel resistorless structures of first-order voltage-mode all-pass filter are presented. Both the presented filter structures are based on FDCCII and exhibit some highly promising signal processing features. Each of the presented structures feature an FDCCII, a grounded capacitor, and an MOS-based active resistor. Presented filters also exhibit high input impedance, which provides cascadability support to the design. The desired all-pass responses are available without any component matching constraint, and the circuits show good sensitivity performance as well. An N^{th}-order voltage-mode all-pass filter and a quadrature oscillator are also presented to verify the applicability of one of the proposed first-order voltage-mode all-pass filters. PSPICE simulations results validate the presented theoretical performance of the filter structures.

References

[1] F Kaçar and Y Özcelep. CDBA based voltage-mode first-order all-pass filter topologies. *J. Electr. Electron. Eng.* 2011; **11**, 1327-32.
[2] C Cakir, U Cam and O Cicekoglu. Novel allpass filter configuration employing single OTRA. *IEEE Trans. Circuits Syst.* 2005; **52**, 122-5.
[3] S Minaei and E Yuce. Novel voltage-mode all-pass filter based on using DVCCs. *Circ. Syst. Signal Process.* 2010; **29**, 391-402.
[4] A Toker, S Ozcan, H Kuntman and O Cicekoglu. Supplementary all-pass sections with reduced number of passive elements using a single current conveyor. *Int. J. Electron.* 2001; **88**, 969-76.
[5] B Metin and K Pal. Cascadable allpass filter with a single DO-CCII and a grounded capacitor. *Analog Integrated Circ. Signal Process.* 2009; **61**, 259.
[6] B Metin and O Cicekoglu. Component reduced all-pass filter with a grounded capacitor and high-impedance input. *Int. J. Electron.* 2009; **96**, 445-55.
[7] MA Ibrahim, H Kuntman and O Cicekoglu. First-order all-pass filter canonical in the number of resistors and capacitors employing a single DDCC. *Circuits Syst. Signal Process.* 2003; **22**, 525-36.
[8] IA Khan and S Maheshwari. Simple first order all-pass section using a single CCII. *Int. J. Electron.* 2000; **87**, 303-6.
[9] S Maheshwari. High input impedance VM-APSs with grounded passive elements. *IET Circ. Devices Syst*. 2007; **1**, 72-8.
[10] S Maheshwari, J Mohan and D S Chauhan. Voltage-mode cascadable all-pass sections with two grounded passive components and one active element. *IET Circ. Devices Syst*. 2010; **4**, 113-12.
[11] B Metin, N Herencsar and K Pal. Supplementary first-order all-pass filters with two grounded passive elements using FDCCII. *Radioengineering* 2011; **20**, 433-7.
[12] J Mohan and S Maheshwari. Additional high-input low-output impedance voltage-mode all-pass sections. *J. Circ. Syst. Comput.* 2014; **23**, 1450077.
[13] J Mohan, S Maheshwari and D S Chauhan. Voltage mode cascadable all-pass sections using single active element and grounded passive components. *Circ. Syst.* 2010; **1**, 5-11.
[14] JW Horng, C Y Tsai, T C Chen and C M Wu. High input impedances voltage-mode first-order filters with grounded capacitors using CCIIs. *Recent Adv. Electr. Electron. Eng.* 2020; **13**, 64-8.
[15] S Maheshwari and B Chaturvedi. High-input low-output impedance all-pass filters using one active element. *IET Circ. Devices Syst.* 2012; **6**, 103-10.
[16] F Yucel and E Yuce. A new single CCII-based voltage-mode first-order all-pass filter and its quadrature oscillator application. *Sci. Iran.* 2015; **22**, 1068-76.
[17] I A Khan, M I Masud and S A Moiz. Reconfigurable fully differential first order all pass filter using digitally controlled CMOS DVCC. *In:* Proceedings of the 8th IEEE GCC Conference and Exhibition, Muscat, Oman. 2015, p. 1-5.
[18] MA Ibrahim, S Minae and E Yuce. All-pass sections with rich cascadability and IC realization suitability. *Int. J. Circ. Theory Appl.* 2010; **40**, 477-88.
[19] MA Ibrahim, S Minaei and E Yuce. All-Pass Sections with high gain opportunity. *Radioengineering* 2011; **20**, 3-9.
[20] B Chaturvedi and J Mohan. Single DV-DXCCII based voltage controlled first order all- pass filter with inverting and non-inverting responses. *Iran. J. Electr. Electron. Eng.* 2015; **11**, 301-9.
[21] B Metin, K Pal and O Cicekoglu. All-pass filters using DDCC- and MOSFET-based electronic resistor. *Int. J. Circ. Theory Appl.* 2011; **39**, 881-91.
[22] S Maheshwari. Analogue signal processing applications using a new circuit topology. *IET Circ. Devices Syst.* 2009; **3**, 106-15.
[23] B Chaturvedi and S Maheshwari. An ideal voltage-mode all-pass filter and its application. *Comput. Commun.* 2012; **9**, 613-23.
[24] P Beg. Tunable first-order resistorless all-pass filter with low-output impedance. *Sci. World J.* 2014; **2014**, 219453.

[25] J Mohan, S Maheshwari and DS Chauhan. Minimum component based first-order all-pass filter with inverting and non-inverting outputs. *ACEEE Int. J. Electr. Power Eng*. 2010; **01**, 32-5.
[26] S Maheshwari. Current-mode circuit with high output impedance for phase-shifting applications. *Int. J. Electr. Comput. Eng.* 2020; **12**, 16-23.
[27] AA El-adawy, AM Soliman and HO Elwan. A novel fully differential current conveyor and applications for analog VLSI. *IEEE Trans. Circ. Syst. II*. 2000; **47**, 306-13.
[28] F Kaçar, B Metin, H Kuntman and O Cicekoglu. A new high-performance CMOS fully differential second-generation current conveyor with application example of biquad filter realization. *Int. J. Electron.* 2010; **97**, 499-510.
[29] CN Lee and CM Chang. Single FDCCII-based mixed-mode biquad filter with eight outputs. *AEU-Int. J. Electron. Commun.* 2009; **62**, 736-42.
[30] B Chaturvedi, J Mohan and A Kumar. A new versatile universal biquad configuration for emerging, signal processing applications. *J. Circuits, Syst. Comput.* 2018; **27**, 1850196.
[31] Jitender, J Mohan and B Chaturvedi. All-pass frequency selective structures: Application for analog domain. *J. Circuits, Syst. Comput.* 2021. https://doi.org/10.1142/S0218126621501504.
[32] Z Wang. 2-MOSFET transresistor with extremely low distortion for output reaching supply voltages. *Electron. Lett.* 1990. **26**, 951-2.