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CMOS Technology for Increasing Efficiency of Clock Gating Techniques Using Tri-State Buffer

Maan HAMEED*, Asem KHMAG, Fakhrul ZAMAN and Abdurrahman RAMLI

Department of Computer and Communication Systems Engineering, Universiti Putra Malaysia, Selangor, Malaysia

(*Corresponding author; e-mail: maan_eng32@yahoo.com)

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Abstract

Clock gating is an effective technique of decreasing dynamic power dissipation in synchronous design. One of the methods used to realize this goal is to mask the clock which goes to the unnecessary to use in specific time. This paper will present a comparative analysis of this clock gating technique in an 8-bit Arithmetic Logic Unit (ALU). The new clock gating method provides a solution to the problems in the existing techniques. The new proposed clock gating technique generating circuit uses tri-state buffer in a negative latch design, instead of OR gate logic. With the same function being performed, this circuit saves more power and reduces area used, irrespective of design performance. The minimum power gain realized 6.4 % percentage in total power consumption by executing 20 MHz frequency. It also used a 0.9 % occupation area. The proposed method was implemented by using ASIC design methodology, and 130 nm standard cell technology libraries were used for ASIC implementation. Furthermore, the architecture of the ALU was created using Verilog HDL language (32-Bit Quartus II 11.1 Web Edition). The simulation was carried out by using the Model Sim-Altera 10.0c (Quartus II 11.1 Starter Edition). Finally, the design will reduce complexity in hardware and similar clock power.

Keywords: Clock gating, power dissipation, dynamic power, low power, tri-state techniques, ALU

Introduction

Improvements in the reduction of power dissipation and in faster device performance are very important. Therefore, there is need for optimal design, which consumes minimum power and requires a minimal area for the highest performance [1]. This need has led to low-power evolution in digital designs. Recently, larger and more efficient batteries are being used to solve the excessive power consumption problem. Therefore, in the modern day, economic and environmental issues have forced researchers to think of improvements and proffer solutions for reducing power consumption and for increasing reliability in digital design. This task was improved in relation with Synopsys and it goals at studying, practicing and evaluating digital design techniques for minimization of power consumption through flexibility of design. This aim is achieved in modern design with the use of high speed digital interfaces. Design flows constructed with Synopsys Electronic Design Automation (EDA) tools and 130 nm technology libraries are currently used for mature products to implement all software and hardware in the target design. This important issue results from rapidity in the growth of battery operated modern digital application devices and other portable communication devices and, in order to tackle this issue, semiconductor devices have been aggressively used to scale up technology creation for the realization of high execution and integration density. Furthermore, the increased density of transistors in high and low frequencies for power dissipation at low frequency during operation has been intensified in every technology generation [2]. It should be noted that in all the portable devices meant for technological improvement, Arithmetic Logic Unit (ALU) is the main part, and represents the heart of any computing device. Moreover, it consumes more power and requires the meeting of demands. To meet these demands, the power efficiency of the ALU target device needs to be improved [3]. This is intended to allow the reduction of power waste through dynamic and static power in the design. Dynamic power consumption is defined as the switching power which is wasted by switching activities, and is explained as;

$$P_{dynamic} = \alpha\, C\, F\, V^2 \qquad (1)$$

where (α) represents the switching activity, (C) represents the capacitance, (V) refers to the supplied voltage, and (F) stands for the frequency of operation design [4]. From Eq. (1), it is witnessed that dynamic power is comparative to the switching activity and the frequency. Therefore, a possible way to decrease power consumption is lowering the parameters that are directly related to dynamic power, because the portable required working at high activity [5].

The problem of power wastage could be solved through clock gating. The reason for using clock gating is grounded in the fact that ALU carries out 2 operational goals, which are arithmetic and logical operations. At this point, it should be understood that the 2 operations could not be carried out simultaneously. Therefore, the clock signal should be switched off in the idle unit, which is inactive at a particular time of operation, and should supply a saved clock signal to the functioning unit. In addition, ALU is divided into 2 functional unit parts. The first one is for the execution of the logical process, while the second one is for carrying out the arithmetic process. Knowledge of the functional parts of ALU has led to improvements in clock gating technique in ALU. In clock gating, clock signals are synchronizing indicators that serve as timing sources for calculations in synchronous digital circuits. It should be noted that achievement of the best quality in this case comes through raising clock frequencies with the help of technology scaling. However, best quality in deep submicron generation could be achieved through increasing parallelism at the architectural design level, and not via raising clock frequencies. Considering the non-stop growth in the complexity of summit-execution Very Large Scale Integration (VLSI), Systems on Chip (SoC) designs, the consequential increase in power dissipation value becomes the main bane to the achievement of the best quality in the system. Clock network complexity results from modern design through increase in the power consumption of the clock, even if the clock frequency cannot be scaled anymore. Therefore, the main function of the aggregate power dissipation in highly synchronous designs, such as microprocessors, is referred to as a clock network. In Xeon Dual-core processor design, a larger part of the total power chip is consumed by a clock allocation network. Thus, innovative clocking methods for lowering the power dissipation of the clock networks are needed for designing digital circuits with great performance and minimum power consumption in the future. The second reason for using clock gating in synchronous designs of clock networks is that it is responsible for higher power consumption, which is up to 40 - 60 %. The proposed design implemented by generating a signal involves clock gating and a tri-state buffer for an 8-bit ALU using 130 nm technologies. Low power consumption has been achieved with clock gating, and the suggested technique has led to improvement in the performance of the ALU.

Related work

Today's high speed modern devices need to operate with low power consumption without sacrificing high performance. It has been discovered through surveying that the processing units of network processors lose much power during their operations. Therefore, reduction of power in these processor elements becomes a great source of concern. However, power lowering leads to reduced switching activities of dynamic power in different traffic volumes [6]. Nevertheless, power consumption reduction methods have been adopted to reduce power at the Register Transfer Level (RTL). Therefore, when power consumption is calculated, a significant power reduction will be observed [3]. Kaur and Mehra [7] invented a new design of counter using clock gated flip-flop. The circuit design is based on a proposed new clock gating flip-flop method to decrease the signal’s switching power dissipation. This has equally led to a decrease in a set of transistors. The suggested flip-flop is used in designing a number of bits in binary counters. A clock gating technique with embedded flip-flop has been proposed to eliminate redundant switching due to the clock and, consequently, reduce power dissipation. Sahni *et al.* [8] discussed the use of encoders and decoders, and how they could improve the power without degradation in the design performance. The technology used here is called gated clock design by using negative latch technique. Here, the gated clock is used to control the 2 modules for encoder and decoder design. Using this technique for the design gives a high reduction in power dissipation, equal to half of the standard design. Shaker and Bayoumi [9] designed a flip-flop utilizing up to 10-bits to design counter and a 14-bit sequence for registration. Improved circuit design of clock gated flip-flop can decrease power dissipation of the clock signal. It works together with no redundant clock cycles, and has decreased the number of transistors to lower the overhead and make it convenient for data signals with the highest switching activity. Benini *et al.* [10] discussed a workable resolution that is compatible with toggling efficient interconnection of flip-flops and their physical state closeness restriction layout. Here, data driven clock gating is integrated into an EDA commercial background design flux, and gating is manually inserted into the RTL [11]. Furthermore, there should be proportional valuations of the clock gating method used in a field-programmable gate array (FPGA), in order to improve the power consumption.

Implementation of 8-bit ALU

The 2 inputs ‘a’ and ‘b’ were 8-bit, and the result was also an 8-bit. The implementation of ALU was conducted through using both negative latch clock gating (CG) and negative latch clock gating using tri-state buffer techniques. The ALU uses 3-bit select lines to select the processes. The implementation of the proposed design is in 2 stages. The microcontrollers/microprocessors with a single module execute arithmetic and logic operations on the basis of integer values, because various operations can be executed using the same hardware. The component that performs these processes is known as the arithmetic logic unit.

Clock gating using negative latch

The output of the negative latch is explained in **Figure 1** as a gated clock (GCLK). The input signal, ‘En’, is given to the negative latch design to achieve the function of clock gating. Therefore, when this En is set to 1, the output of the (GEN) latch is 0. In this case, XNOR provides the output signal (x) to 0 and provides the primary logic for the clock creation of the controlling design or latch [3]. Moreover, when the next clock pulse arrives, within the following clock, the (GEN) turns to 1 and thus creates the second logic for clock generation. The second logic is designed as the AND gate, which is the purpose of (GEN) and global clock (CLK). The output of AND gate represent by the clock pulse named (GCLK), and this signal supports the target design. As GEN is 1, so x is also equal to 1. The OR gate gives an output (CCLK) as high as 1 until ‘En’ is low (0). This indicates that the latch will hold its state without any switching activities. The full design is shown in **Figure 2**.

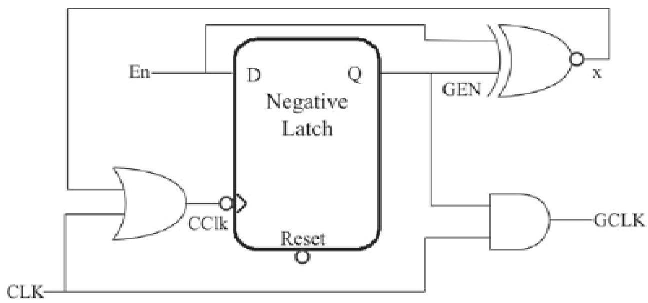


Figure 1 Clock gating negative latch.

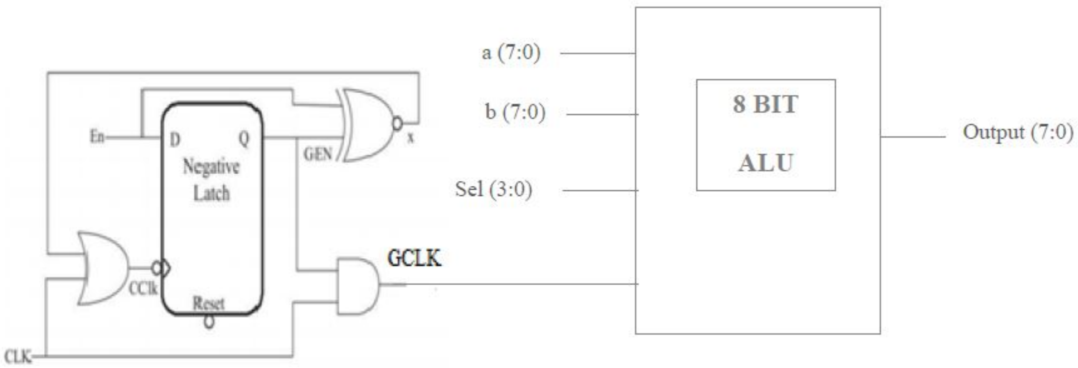


Figure 2 Block diagram of 8-bit ALU with negative latch clock gating.

New approach using tri-state

A new method of improving power consumption was suggested. This method was implemented using a tri-state buffer, as shown in **Figure 3**. The proposed design is a new method for improving clock gating, which will save more area and power [12]. The new signal gated clock created by using a tri-state buffer instead of an OR-gate will improve the design performance more than using an OR-gate for power dissipation and area saving [13]. During the high impedance for tri-state output (GEN), the latch out depends on the previous state for the latch to control (GCLK). The base concept of this manner is that, in the traditional clock gating, using a negative latch synthesizer tool in Synopsys power compiler deals with the logic gates as registers. This implies using a clock and consuming power and area. However, in the new approach, the synthesizer tool in Synopsys power compiler deals with the tri-state as wires. The essential achievement of this work is to improve the novel clock gating method with low power consumption and to increase the performance of the system, because increasing power dissipation makes the design unreliable. Therefore, to manage the switching activity, the new tri-state based clock gating technique was proposed with low power consumption implemented in an 8-bit ALU. The size of an ALU can be easily modified by 16 bits, 32 bits, and 64 bits. This is due to the fact that power is directly proportional to the voltage and the frequency of the clock. Moreover, this technique can be used in different designs, because the technology used in this way generates clock output latch when the tri-state is off depending on its previous state, without depending on the type of design used. Comparative analysis for all types of power shows that the suggested method impacts power consumption as a decrease, in comparison to the conventional method.

In [13], a tri-state was used instead of a selector to choose one operation and block other operations in order to save more power. Meanwhile, the newly proposed method used to improve the quality of clock gating by reducing power consumption compares well with previous results using the same design by decreasing the complexity of the design. Moreover, the technique in [13] is dissimilar to other digital design like Huffman, because not all digital designs have selectors.

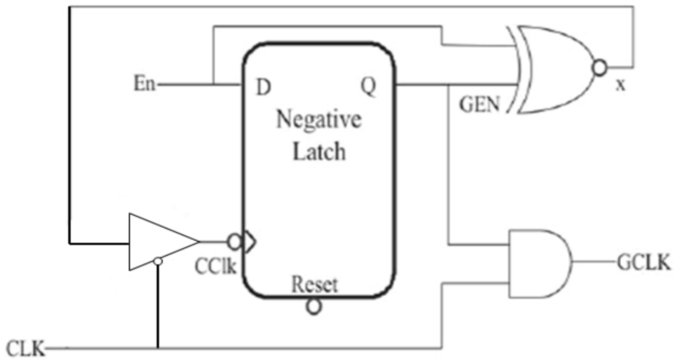
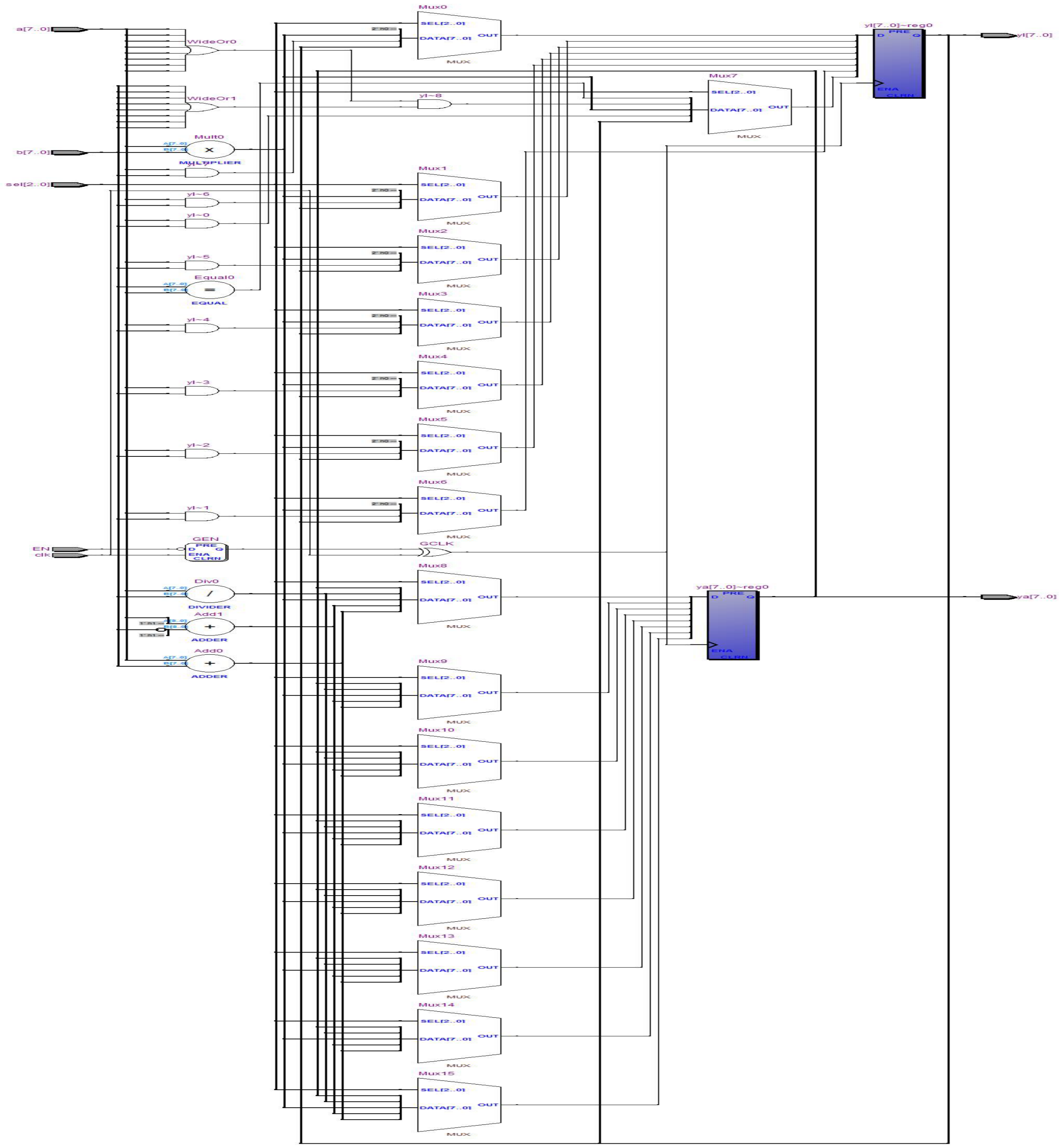


Figure 3 Clock gating using tri-state.

Simulation and results

The simulation is done using the ModelSim-Altera 10.0c (Quartus II 11.1 Starter Edition) and the Mentor Graphics ModelSim-Altera10.0c (Quartus II 11.1). This simulator is a source-level investigation tool which allows the designer to prove HDL code line by line. The input is given during the test bench and the output is correspondingly shown by a simulated waveform. Binary inputs of ALU are given by ports 'a' and 'b'. En works as an enabled signal; when the value of 'En' is set to high, the simulation waveform shows that a logic operation has to be performed, while, when the 'En' set is low, the target unit of execution from the ALU is an arithmetic unit. **Figure 4** shows the RTL viewer of an 8-bit ALU using Altera10.0c (Quartus II 11.1). **Figure 5** show the waveform validation of ALU using the ModelSim-Altera 10.0c (Quartus II 11.1 Starter Edition). **Figure 6** clearly shows the hold state waveform of the tri-state.



Figures 4 RTL viewer of the 8-bit ALU.

Figure 5 Simulation result of the ALU using tri-state.

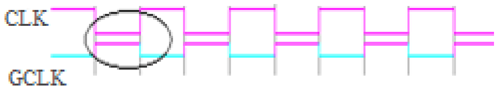


Figure 6 Hold state wave form.

Proposed design operations

The proposed ALU consists of 2 inputs, an 8-bit long with a select line, and a 3-bit long for selecting arithmetic or logic process. ClK signals AND with 'GEN' and incorporates a tri-state buffer to improve the outcome of clock gating by saving more power consumption. Arithmetic logic processes that should be executed in the proposed design are listed in **Table 1**.

Table 1 Proposed ALU operations.

No.	Opcode value	Operation
1	000	(A + B)
2	001	(A – B)
3	010	(A * B)
4	011	(A/B)
5	100	(B – A)
6	101	(A&B)
7	110	(A&&B)
8	111	(A==B)

Clock gating power analysis

By using enabled clock gating, the power consumption decreases [14]. **Table 2** shows the provision of power dissipation of an 8-bit ALU with a negative latch using 130 nm technologies. There are 2 kinds of power consumption: static and dynamic power consumption [15]. This work discusses the dynamic power dissipation which is directly proportional to the magnitude of frequency for the clock signal and inversely proportional to the period of the clock. The period of the clock is equal to the inverse of the frequency applied to the design. When executing any ALU process with a clock period of 50 ns and where clock gating is under consideration, a total power of 0.0389 mW, a dynamic power of 0.0382 mW, and a static power of 0.0006 mW are required. When we implement an ALU with a period of 10 ns, a total power consumption of 0.2351 mW, a dynamic power of 0.2344 mW, and a leakage power of 0.0007 mW will be required for the design. Moreover, the area occupation in this design, estimated from the Synopsys power compiler report, is (5.1091×10^{-9}) mm^2. From Eq. (1), the dynamic power consists of internal power and switching activity, as shown in **Table 2**.

Table 2 Negative latch clock gating power.

No.	Frequency (MHz)	Internal power (mW)	Switching power (mW)	Dynamic power (mW)	Static power (mW)	Total power (mW)
1	20	0.0385	0.0078	0.0382	0.0006	0.0389
2	40	0.0609	0.0156	0.0765	0.0006	0.0772
3	60	0.0979	0.0287	0.1266	0.0007	0.1275
4	80	0.1464	0.0451	0.1914	0.0007	0.1923
5	100	0.1763	0.0781	0.2344	0.0007	0.2351

Moreover, the Synopsys Design Compiler (DC) is defined as a tool for the synthesis of Synopsys. The key to appropriate power analysis tools is the automatic reducing power method. This way benefits designers to match power statements without degrading outcomes or time of design. The Synopsys power compiler is a tool used to automatically reduce power consumption at the Gate Level (GL) and RTL of a design. At the system elaboration mode of RTL, the power compiler performs automatic clock gating to decrease the power dissipation. After uploading a full design in the Synopsys tool, with specific design restrictions, the power compiler implements improvements for the area, timing, and power with each other [16]. **Figure 7** shows the input requirements for the Synopsys tool to produce the netlist.

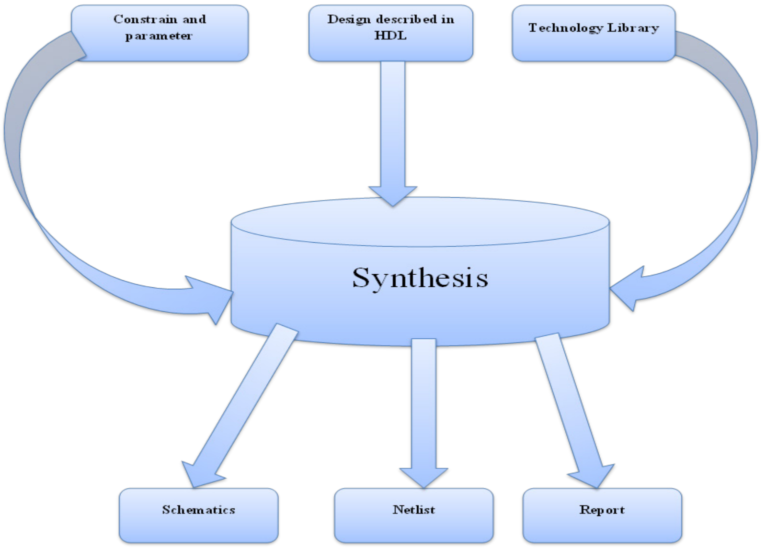


Figure 7 Inputs and outputs of the synthesis process.

Switching the logic gate by using a tri-state buffer leads to saving more power. The proposed design is executed at different scales of frequency. The power consumption will be according to what is shown in **Table 3**. It is possible to see clearly that the new design with a tri-state consumes less power than the previous state, and there will be an increase in the quality of clock gating [13]. When executing any ALU process with negative latch clock gating using a tri-state buffer in a clock period of 50 ns with the use of clock gating, a total power of 0.0364 mW, a dynamic power of 0.0358 mW, and the same static power is required. In executing a design with a period of 10 ns, a total power consumption of 0.2096 mW, a dynamic power of 0.2091 mW, and a leakage power of 0.0005 mW are required for the design. Moreover, the area occupation in this design, estimated from the Synopsys power compiler report, is 5.0633×10^{-9} mm^2. From Eq. (1), the dynamic power consists of internal power and switching activity, as shown in **Table 2**.

Table 3 Power consumption using tri-state.

No.	Frequency (MHz)	Internal power (mW)	Switching power (mW)	Dynamic power (mW)	Static power (mW)	Total power (mW)
1	20	0.0291	0.0066	0.0358	0.0006	0.0364
2	40	0.0583	0.0133	0.0716	0.0005	0.0721
3	60	0.0976	0.0210	0.1186	0.0006	0.1192
4	80	0.1466	0.0267	0.1733	0.0006	0.1739
5	100	0.1738	0.0353	0.2091	0.0005	0.2096

Power consumption using a tri-state is presented in **Table 3**. It was clearly observed that there was a reduction in power consumption using the tri-state buffer. Furthermore, the 8-bit ALU was implemented at a 10 GHz clock frequency, and achieved 309.9743 mW. In [2], an 8-bit ALU was applied in different libraries to estimate power consumption, as shown in **Table 4**, with all power estimations in mW. Moreover, when this work was modified to a 32-bit ALU to perform a quantitative analysis of the power with the proposed tri-state buffer, it was observed that the total power consumed 0.5864 mW, using a 32-bit ALU in 20 MHz. It was clearly seen that there was a difference in total power consumption when the size of ALU was extended.

Table 4 Comparison of power consumption for different technology libraries.

Frequency (GHz)	Clock Gating technique	Technology 130 nm	Technology 90 nm	Technology 65 nm	Technology 45 nm
10	negative latch	309.9743	1200	2042	2011

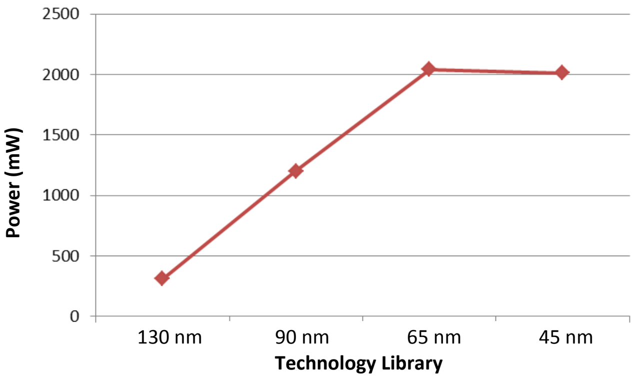


Figure 8 Variation of power consumption depending on library scale.

In **Table 4**, Synthesis process Gate-level optimization operates on generic netlist generated by logic gate synthesis to create a netlist technology-specific. Important processes are implemented during the synthesis process [17]. These processes are Mapping, Delay Optimization, and Design Rule Fixing. **Figure 8** shows the variation of power consumption using different library scales; the differences in the values of power consumption depend on 3 main parameter inputs for the synthesis process, as shown in **Figure 7** (Constrains for design, Design described in HDL, and Technology library). Moreover, the environment used to operate the design is very important in power analysis. The procedures of power analysis are summarized by converting the frequency applied to the design into time per nanosecond. Then, the parameters of the Saltera 130 nm technology library used for power analysis are set to select the top-level design generated reports for all types of power consumption (Internal, Switching, Dynamic, Static, and Total power), in addition to area occupied by the design. In **Table 3**, the result of power analysis with the same criteria in a conventional negative latch and the same scales of frequencies implemented on an 8-bit ALU shows that the proposed design using a tri-state buffer consumes less power compared to the conventional state, meaning that the proposed design is better than the conventional negative latch (**Figure 9**).

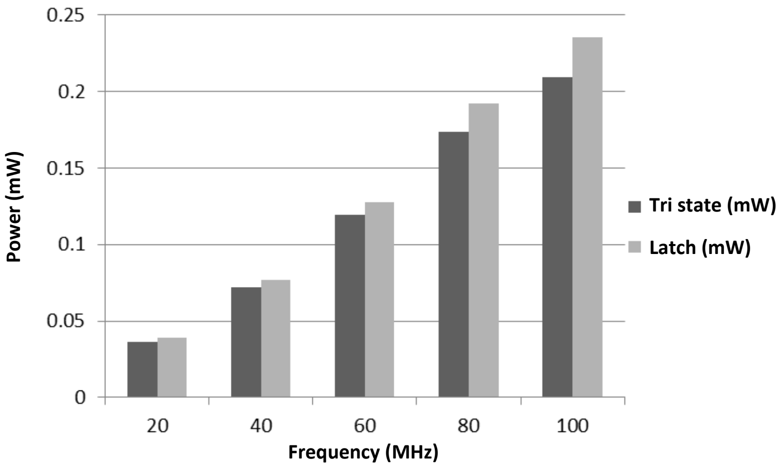


Figure 9 Power variations with frequency.

Conclusions

The newly proposed technique will save more area and power by avoiding the idle parts and reducing the complexity of a design. The key contribution of this work is that it will lead to the development of a new technique of clock gating, with reduced area occupation and optimization of the quality of the system. The increment in dynamic power dissipation causes the design to be unreliable. Therefore, to manage the switching power, several methods are considered and investigated in order to decrease it. A newly suggested way of using a switching tri-state buffer instead of an OR-gate in a negative latch clock gating technique with low area occupation and power dissipation was also proposed and implemented. A comparative power analysis showed that the suggested way results in the dynamic power decreasing to as low as 6.4 %, in comparison to the conventional negative latch. The proposed design will reduce the hardware leads so as to reduce the complexity of circuit and the area occupation to about 0.9 %. All the analyses of power consumption were done on an 8-bit ALU with process variation parameters.

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